Adding Analog and Mixed Signal Concerns to a Digital VLSI Course

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Abstract

This paper describes a new approach to teaching a VLSI Systems Design course that integrates basic analog and mixed-signal design considerations into what was previously an all-digital course. VLSI chips increasingly contain both analog and digital components, making it important for students to have some familiarity with both topics. The revised course integrates analog concerns by building on the standard techniques for digital integrated circuit design and extending this coverage to include digital-analog and analog-digital conversion. Students design these elements in the course laboratory, producing a complete chip that is submitted for fabrication at the end of the semester. The resulting experience gives students a strong grounding in digital integrated circuit design, an understanding of some important analog concepts, and an appreciation for the relationship between digital design and analog design.

1. Introduction

Very Large Scale Integration (VLSI) is the enabling technology for an ongoing revolution in computers, communications, and electronics. The importance of this key technology makes a VLSI Design course an essential ingredient in a competitive Electrical and Computer Engineering curriculum. Traditional VLSI Design courses focus primarily on digital integrated circuit design. Analog integrated circuit design is usually covered in a separate course, often at the graduate level. The problem with this approach is that the day of the purely digital chip is passing – most new chip designs include both analog and digital components. For example, it is now common for digital chips to integrate digital-analog (D/A) and analog-digital (A/D) converters to interface with the analog "outside world". Moreover, large "mixed signal" communications and consumer electronics "system on a chip" designs combine large blocks of both digital and analog circuits. Finally, shrinking transistor geometries require that digital chip designers consider circuit-level issues which were formerly only of concern in analog chips.

This paper describes an effort to meet this challenge by augmenting a digital VLSI course with analog and mixed-signal concerns. Since the two topics share a common foundation (e.g., layout processing, device physics, parasitics, etc.), our approach has been to include small "digressions" into analog design at different points during the course, along with laboratory experiences which reinforce both digital and analog design concepts. The result is a course in which students gain an appreciation of analog concerns as well as a broad-based grounding in digital integrated circuit design.

This paper is organized as follows: Section 2 describes the objectives of the modified course and its general organization; Section 3 details the analog material that is added to the course, in both the lecture and the laboratory; Section 4 describes our experience teaching the modified course during the Fall 2001 semester; Section 5 provides conclusions and suggestions for future work.

2. Course Overview

VLSI Design courses became popular in the early 1980s, following the publication of Mead and Conway's pioneering book, *Introduction to VLSI Systems*[1]. This book introduced the "tall, thin designer" paradigm – the idea that VLSI systems designers needed expertise at several different levels of abstraction, starting with CMOS layout, devices physics, transistor and parasitic characteristics, and working up through the circuit design, logic design, and architectural levels. While the last 20 years have brought dramatic changes in technology, CAD tools, and design methods, this bottom-up approach to teaching has proven to be effective and remains in use today.

At the same time, Mead and Conway recognized the value of fabricating and testing student design projects, and pioneered the use of *multi-project chips* to fabricate chip prototypes in a cost-effective way. Again, this approach has proven to be popular and effective, and the MOSIS Educational Program[2] has made this option available to colleges and universities throughout the United States.

The introductory VLSI Design course at Lafayette College, *ECE 425 – VLSI Circuit Design* follows both of these trends. The goals of this course are to provide students with an understanding of VLSI technology and familiarize them with design methods at the layout, logic, and architectural levels of abstraction. A laboratory component emphasizes design experience, and students complete a small chip design that is fabricated by MOSIS.

Prior to the Fall 2001 semester, this course focused exclusively on digital integrated circuit design. In revising the course to include analog concerns, we had the following goals:

1. To focus on analog material that will also be useful to engineers primarily involved in digital design.
2. To teach the analog concepts as an extension of the analysis and design methods used in digital integrated circuit design.
3. To continue to have a strong focus on digital design, and remove a minimal amount of digital design material to make room for the analog coverage.
4. To lay the foundation for further study in analog chip design without duplicating an existing analog design course.

To meet these goals, the added analog material focused around the topic of *data conversion* – conversion from digital values to analog values, and vice-versa. This is highly useful material and can be taught as an extension to digital integrated circuit design.

Moreover, it provides the opportunity for a challenging set of laboratory design problems that mix both digital and analog design.

Table 1 shows the outline of the revised course, with the new topics shown in boldface. To make room for this material, some advanced coverage on VLSI system design was removed from ECE 425 and moved to a follow-on course, *ECE 426 – VLSI System Design*. A key part of the student experience in ECE 425 is the course project, which involves the design of a full chip that implements a 4-bit Successive Approximation A/D Converter. These chips are submitted for fabrication by MOSIS at the end of the fall semester and tested during the spring semester as part of the ECE 426 laboratory.

Lecture Topic	**Laboratory**
CMOS Processing	Schematic Editing / Simulation
Device Physics; MOS Transistor Characteristics	
Parasitic Components	Basic Gate Layout
Layout and Design Rules	
Extraction, Simulation, and Layout Verification	Extraction/Simulation/LVS
Hierarchical Layout	
Voltage-Scaling D/A Conversion	**Layout Mini-Project: 4-bit Voltage Scaling DAC**
ASIC Layout Styles: Std. Cells, Gate Arrays, FPGAs	
Combinational Logic: Gate Design and Layout	
Comb. delay and power dissipation; testing	
Comb. Design with HDLs & Logic Synthesis	HDL Design (Combinational)
Sequential Logic: Latch & Flip-Flop Design	
Sequential Circuits and Clocking Schemes	
Sequential Design with HDLs & Logic Synthesis	HDL Design (Sequential)
Sequential Testing & Design for Test	
Successive-Approximation A/D Conversion	**Final Project: 4-bit Successive Approximation ADC**
Clocked "Auto-Centering" Comparators	
Digital VLSI System Design	
Analog VLSI Overview	

Table 1 – ECE 425 Organization

3. Analog Concepts Introduced in ECE 425

This section provides more detail about the analog material that was added to the course. Each topic is presented in the context of a specific design problem which ties into a laboratory experience and strongly reinforces the class presentations.

3.1 The Voltage-Scaling D/A Converter

A multiple-bit digital signal can be converted to an analog signal in a number of different ways. The *voltage-scaling* approach is popular because voltage-scaling D/A converters (DACs) are easy to implement in digital integrated circuit processes and have monotonic

output characteristics. A voltage-scaling DAC is essentially a large string of identical resistors which form a voltage divider. For an *n*-bit digital input , this divider produces 2^n evenly-spaced voltages. CMOS "transmission gate" switches are used to connect *one* of these voltages to the DAC output at any given time. These switches are connected to a decoder so that the lowest digital value selects the lowest divider voltage and increasing digital values select successively higher divider voltages. The result is an analog output that is proportional to the numerical value of the digital input signal.

Figure 1 shows the organization of a 4-bit voltage-scaling DAC. In this circuit, the resistor chain is folded into four columns to make the circuit layout fit into a smaller space.

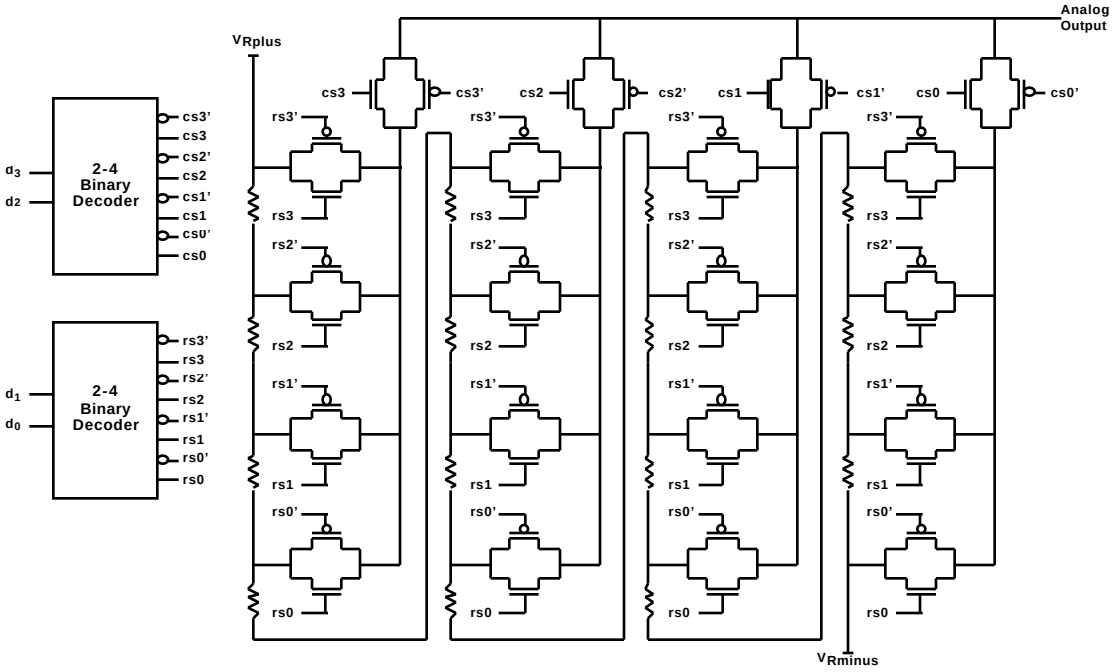

Figure 1 – 4-bit Voltage-Scaling DAC

The concept of voltage-scaling D/A conversion is the first analog topic presented in ECE 425. It is presented after students have learned the concepts of integrated circuit processing and fabrication, transistor operation, parasitic components, basic logic gate design and layout, and hierarchical layout. This provides a foundation for explaining the operation of a voltage-scaling DAC even though the emphasis of the previous coverage was on digital circuits. Parasitic components provide the basis for creating a chain of resistors. Transmission gates have been covered from a digital context, but the use of a transmission gate to pass an analog value is easily understood as an extension of its digital use. Students can therefore easily grasp the operation of the circuit without a large digression from the material normally presented in a digital chip design course.

The voltage-scaling DAC also provides an interesting and challenging hierarchical design problem, which the students attack in the laboratory. Hierarchical layout concepts which were taught for digital chip design are equally applicable to this analog design problem. In

the laboratory, students first design a leaf cell that consists of a polysilicon resistor and transmission gate. These cells are used to create four higher-level cells that implement the four columns of the voltage divider and are combined with all-digital decoder cells to form the complete design. Creating this layout gives students a strong experience in hierarchical design and greatly strengthens their layout skills in both digital and analog circuit design. As the circuit is designed, the cells in the hierarchy are extracted and simulated using a combination of digital and analog simulators.

3.2 Successive-Approximation A/D Conversion

Successive-Approximation A/D conversion is a popular and economical way to convert analog signals to digital signals. It is a good example of a mixed-signal circuit that combines analog and digital circuits to perform its function. In ECE 425, this circuit is presented about two-thirds of the way into the course and is used as a final design project in the laboratory.

Figure 2 shows the block diagram of a typical successive approximation A/D Converter. It consists of a D/A converter, a comparator, and an estimation circuit known as a *successive approximation register (SAR).* In operation, the SAR generates an *estimate* digital value that is converted to an analog voltage V_E by the DAC and passed to the comparator, which determines whether the estimate V_E is greater than the analog input V_I. By using binary search, the SAR can perform an *n*-bit conversion in *n* clock cycles.

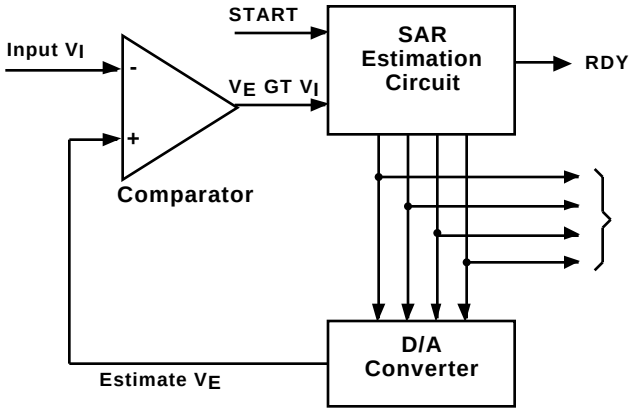

Figure 2 – Successive Approximation A/D Converter

To create this circuit in the laboratory, students use the D/A converter which they designed previously, a comparator circuit that is provided by the instructors, and a SAR that they design using the Verilog Hardware Description Language (HDL) and synthesize into a standard-cell layout block using a collection of synthesis and physical design CAD tools. They then assemble these blocks to form the complete circuit, simulate it to verify its proper operation, and place it in a pad frame so that it can be fabricated as a MOSIS "tiny chip."

3.3 Clocked Auto-Centering Comparator Design

As mentioned earlier in this section, the A/D converter requires a comparator circuit that is provided to students by the instructor. While many comparator designs are based on high-gain differential amplifiers, the design of such a circuit is beyond the scope of this course. Instead, an alternative design is used: the clocked offset-canceling comparator[3].

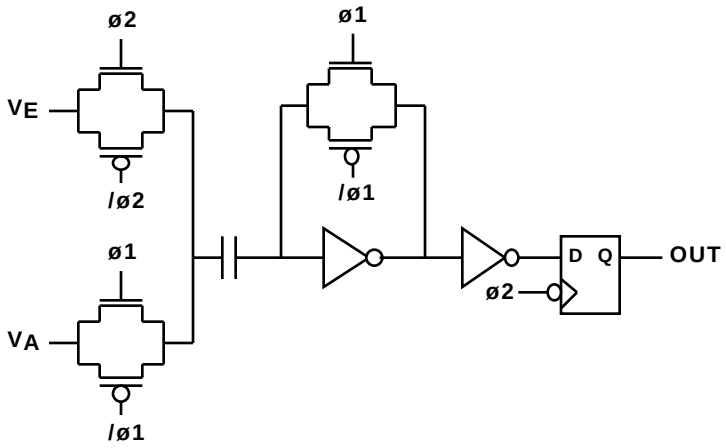

Figure 3 – Clocked Offset-Canceling Comparator

Figure 3 shows the basic structure of this circuit, which consists of two inverters (used as amplifiers), three transmission gates, and a D flip-flop. It operates in two phases as controlled by clock signals ø1 and ø2. During the *reset* phase (when ø1 is high) the input and output of the leftmost inverter are connected, forcing its output to the center of its output range. At the same time, voltage V_A is connected to the input terminal of the capacitor, so that the capacitor charges to the *difference* between V_A and the centered voltage. During the *evaluation* phase (when ø2 is high), the connection between the inverter's output and input is broken and the input terminal of the capacitor is connected to V_E. Since the capacitor conserves charge, the input voltage of the inverter will shift higher or lower depending on whether V_E is less than or greater than V_A. This small shift on the input of the inverter will result in a much larger offset on the inverter output, which is connected to a second inverter that further amplifies and inverts this value to create a strong digital "1" if $V_E > V_A$ or "0" if $V_E \leq V_A$. This result is then latched into a flip-flop before the next reset phase begins. A separate clock generation circuit (not shown) is used to produce these clock signals in the circuit that is provided to the students.

While the operation of this circuit appears complicated, it can be presented in class using extensions of digital IC design concepts. Specifically, the use of transmission gates has already been covered in digital design and also in the voltage-scaling DAC. The use of capacitors and pre-charging are covered in class discussions of dynamic logic. By extending these concepts, the presentation of this design in class reinforces students' understanding of the original digital techniques while showing how these techniques can be applied in analog circuits.

3.4 A View Ahead: An Overview of Advanced Analog Design

While ECE 425 includes analog concerns as an extension of digital integrated circuit design, it only scratches the surface of more advanced analog topics. A lecture at the end of the course briefly explores these topics and summarizes the building blocks of analog integrated circuits (e.g. current sources, current mirrors, amplifiers, switched-capacitor filters, etc.). In addition, it describes current trends in analog and mixed-signal design. Interested students can then take a newly-developed course in Advanced Analog Integrated Circuit Design to study these topics in more detail.

4. Results

The new version of ECE 425 was taught for the first time in the Fall 2001 semester. The new lab experiments including the D/A and A/D converter designs were developed as the course progressed and were successfully completed by all of the students in the class. On the A/D Converter final project, students worked in eight groups of one or two. Seven of the eight chip designs completed by these groups were submitted to MOSIS for fabrication in January 2002; fabricated chips were returned in March 2002 for testing. Figure 4 shows one of these chip designs, created by Lafayette student E. Thomas. Student response to the course has been enthusiastic, and many of the students in ECE 425 have enrolled in ECE 426 to participate in chip testing.

5. Conclusion

This paper has described the successful inclusion of analog concerns in a digital VLSI Design course, primarily through added coverage of D/A and A/D conversion. The resulting course continues to give students a strong grounding in digital VLSI Design while adding an understanding of basic analog and mixed-signal issues and a detailed understanding of conversion circuits. Future work will include additional revisions to the laboratory experiments, a closer integration of analog and digital topics in the lecture notes, and the exploration of additional design projects, for example higher-resolution conversion circuits or PLL-based frequency synthesizers. The lecture notes and laboratory materials used in this course are available on the web at http://foghorn.cadlab.lafayette.edu/ece425/.

References

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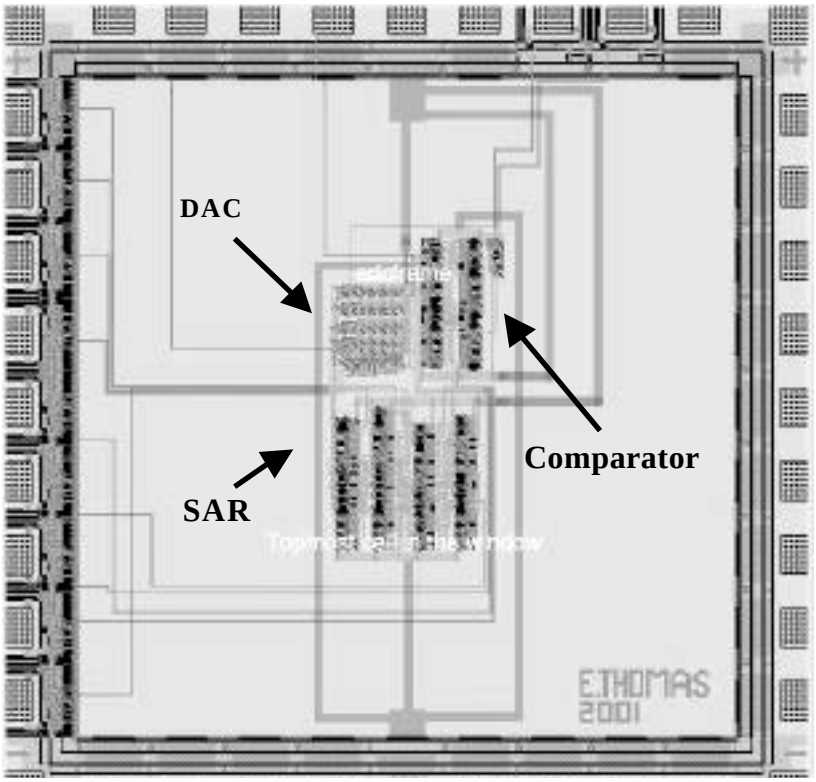

Figure 4 – Student A/D Converter Chip