An Advanced Digital Systems Course: ASICs and HCPLDs

Gregory L. Moss
Purdue University

Abstract

Industry analysts predict that application-specific integrated circuits (ASICs) will be the primary medium for the design of electronic products by the turn of the century. We are in the midst of an ASIC revolution. Many basic product objectives may be unattainable without using ASICs. ASICs provide many system design benefits including improvements in performance, reliability, power, system size, cost, and market competitiveness. There are several different ASIC methodologies available for system design and implementation. Full custom, cell-based, array-based, and programmable logic are the major choices; each with its own set of advantages and disadvantages to be weighed. This new revolution in digital logic design is made possible through electronic design automation tools that run on workstations and desktop personal computers. The computer aided engineering tools that are available today are having a significant impact upon the design of digital systems. With these powerful computer tools, industry is discovering that engineers can readily improve their productivity in creating digital designs.

Programmable logic devices (PLDs) allow designers to quickly and easily develop new digital circuits of moderate complexity for specialized applications. The low cost and availability of high-capacity programmable logic is changing the face of the design process by replacing perhaps hundreds of standard ICs with a single HCPLD chip. With PLDs, the designer is able to specify the necessary function or functions that the devices must produce. HCPLDs also make it possible for students to implement larger and more complex logic designs in the lab.

The explosive growth rate of ASICs forms an imperative for engineering and engineering technology schools to provide appropriate educational experiences for their students. Several options are available to institutions. This paper will look at some of the options and will describe an Advanced Digital Systems course taught at Purdue University in Electrical Engineering Technology.

ASIC Issues

ASIC technology provides a number of advantages in digital system design to industry. Their use will typically permit expanded functionality for a product in a smaller space using fewer parts, thereby decreasing power and cooling requirements overall and increasing system reliability. System performance gains can often be achieved through higher levels of integration attained with ASICs. Time to market for new products can be drastically reduced with some types of ASICs, resulting in the potential for greater profits to the companies who choose to take advantage of this technology,

ASICs, like any technology, are not without a downside. Unfamiliar technology always has many pitfalls (not to mention a learning curve and fear of the unknown) which can engender a schedule risk for the product. The complexity of these highly integrated chips pose some very significant design debugging, development, and production testing issues. Some categories of ASICs can have very high non-recurring engineering (NRE) charges to create the customized chip layout which must be amortized over very large quantities to achieve the necessary economics for a profit. Design changes late in the development cycle can be very costly with some types of ASICs.

Although some of the ASIC disadvantages can be discouraging at first glance, many of the concerns are being resolved. Design tools are maturing, becoming less expensive, and are easier to use. These tools enable designers to cope with ever-increasing demands for added product functionality, features, and complexity. Larger wafer sizes and better yields are resulting in lower production costs. Today, the advantages of using ASICs far outweigh the disadvantages.

Economic and performance considerations as well as tool capability and process fabrication quality have evolved to the point where consideration of ASIC design is now commonplace in an ever-increasing number of electronic system designs, The inclusion of ASIC technology in their design delivers such significant advantages that no designer today can honestly say that he or she is proficient and thorough at developing an electronics solution to whatever problem is being approached without an understanding and knowledge of the options afforded by the incorporation of ASIC technology.

ASIC Technology

There are four major methodologies or types of ASICs including full custom, standard cell, gate array, and programmable logic, Each methodology has fundamental differences in levels of integration, gate count, design tools and procedures, design verification issues, and development and production costs. The selection of an appropriate methodology for an application should be based on its ability to satisfy all design objectives while providing the shortest possible time to market with the lowest development and production costs.

A full custom ASIC has each component and interconnect in the design individually drawn and manually positioned in the circuit layout. Custom masks are needed for all layers in the chip's fabrication. The major goal is to obtain the best possible performance with the smallest possible chip size. This top of the line design choice has the highest NRE costs and requires the longest design cycle. Time to market should not be the most critical design issue. Very high volumes are needed to be a cost effective solution.

A standard cell ASIC uses pre-defined functional blocks called cells which are actually performance-optimized transistor-level designs for a specific semiconductor process that are stored in a library, The symbols of the desired cells are used to draw the circuit schematic for the design which is then used to create a computer-generated physical layout of the chip. The NRE cost and design cycle time for standard cell ASICs are lower than for full custom. The trade-off is generally a lower performance capability and a lower density.

A gate array ASIC is fabricated on preprocessed wafers that contain columns of unconnected transistor arrays (gates) surrounded by 1/0 pads. The desired logic functions are created in the final fabrication steps on the wafer where the metal layers (interconnections) are deposited. Lower NRE costs and shorter fab cycles are achieved since only the final 2 or 3 IC fabrication masks are custom designed. The performance of gate arrays is difficult to predict since it is dependent upon the final placement and routing of the design, Gate usage is

generally inefficient since the wafers are prefabricated in a range of discrete sizes with a fixed number of available gates. The customer ends up paying for any unused gates on the chip.

Programmable logic provides a relatively low risk entry into ASIC technology and is currently experiencing the fastest growing market share. The high-capacity programmable logic devices (HCPLDs) available are rapidly increasing in complexity, density, and performance. Due to its user programmability, it is generally considered to have no NRE cost but the highest cost per gate. Programmable logic usually provides the capability for a very fast time to market advantage for products. In addition to final product applications, HCPLDs are frequently employed for proof of concept prototyping of new designs and as an initial market entry strategy. HCPLDs are available in two major architectures, complex programmable logic devices (CPLDs) and field programmable gate arrays (FPGAs).

Various semiconductor process technologies are available for ASIC design implementation including CMOS, ECL, BiCMOS, and GaAs. Selection of the fabrication process is dependent upon the design goals of the application. CMOS is the most popular technology today due to its low power, ease of design, and ever-improving performance. ECL is used in applications needing very high speed performance but has the drawbacks of high power consumption and low density. BiCMOS represents a compromise which results in a speed/power performance that is better than either process alone. GaAs currently represents a small percentage of the ASIC market but it has the potential of becoming a mainstream ASIC process technology for ultra-high performance applications.

Packaging decisions must also be made for an ASIC. Packaging must be treated as an integral part of the design process in order to realize the full benefits of the chip inside. Some of the considerations for package selection include chip size, pin count, chip heat dissipation, electrical performance, package material, package footprint, chip-to-package and package-to-PCB interconnect, and cost.

Course Options & Content

Chip fabrication services (for educational institutions as well as industry) are available through MOSIS to implement standard cell or full custom ASIC designs but the turn-around time of approximately 8 weeks can be a major logistical problem. Some semiconductor fab houses and fab equipment manufacturers have also expressed interest in supporting university student laboratories but providing clean room facilities can still be a problem, Student laboratory projects relating to ASIC applications can most easily be accomplished using HCPLDS. The two principal companies are Xilinx, Inc. (mainly FPGAs) and Alters Corporation (CPLDs). Both companies have University programs that provide free support including components, software tools, and associated hardware.

Advanced Digital Systems, a junior/senior elective, is offered by the Electrical Engineering Technology Department at Purdue University in West Lafayette, Indiana. This course, which has been taught for 3 years, examines general digital design techniques and topics, with a specific focus on digital system implementation using ASICs. ASIC issues, trade-offs, economics, and design decisions are discussed in lecture. Students design and test ASIC system prototypes using Alters's MAX7000 series CPLDS in the laboratory. The EPM7032 in a 44-pin PLCC package is the main chip used for the lab projects. This CMOS EEPROM technology device contains 1200 "available gates" in 32 macrocells. The 7032 has a maximum of 36 user 1/0 pins. Students are currently assigned 7 design projects in lab, including one project that requires two of the 7032 chips to complete and a final project that may be implemented in a 68-pin EPM7096 (that contains 96 macrocells). This series of chips goes up to 10,000 "available gates" in 256 macrocells with 164 user 1/0 pins. Alters's MAX+plus 11

programmable logic development system and software provide the necessary tools for design entry, compilation, simulation, and programming in an integrated Windows-based environment, Designs are entered using modular design techniques in a hierarchical fashion with any combination oftext-based blocks (Altera Hardware Description Language), schematics, or waveforms. EDIF netlist files, VHDL, and Verilog HDL are also supported by the software but are not currently used in the lab. An introduction to VHDL is also presented in lecture.

References

1. Altera 1995 Data Book. San Jose, California: Ahera, 1995,
2. Alters MAX+plus II AHDL Manual. San Jose, California: Alters, 1994.
3. Alters Web page. http://www.altera.com
4. Chan, Pak K. & Mourad, Samiha. Digital Design Using Field Programmable Gate Arrays. Englewood Cliffs, New Jersey: Prentice Hall,1994.
5. Huber, John P. & Rosneck, Mark W. Successful ASIC Desire the First Time Through. Van Nostrand Reinhold, 1991.
6. Jenkins, Jesse H. Designing with FPGAs and CPLDs. Englewood Cliffs, New Jersey: Prentice Hall, 1994.
7. MOSIS Web page, http://www.isi.edu/mosis
8. Oldfield, John V & Dorf, Richard C. Field Programmable Gate Arrays. New York: John Wiley & Sons, 1995.
9. Pellerin, David & Honey, Michael. Practical Desire Using Programmable Logic. Englewood Cliffs, New Jersey: Prentice Hall, 1991.
10. Schroeter, John. Surviving the ASIC Experience. Englewood Cliffs, New Jersey: Prentice Hall, 1992.
11. Xilinx Programmable Logic Data Book. San Jose, California: Xilinx, 1995.
12. Xilinx Web page, http: //www.xilinx.com

GREGORY L. MOSS

Gregory L. Moss is an Associate Professor of Electrical Engineering Technology at Purdue University, West Lafayette, Indiana. He holds a BSEE from Purdue& an MA in post-secondary education from Ball State University. His industrial experience includes digital IC product development, manufacturing engineering, & industrial training with Delco Electronics. His interests include digital systems, PLD & ASIC technology, curriculum development, and educational technology.