A Radio Frequency Integrated Circuit Design Course
With State-of-the-Art Technology Support from Industry

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I. Introduction:

The dawn of the 21st century is witnessing a tremendous demand for wireless communications and information services, such as Personal Communications Services (PCS—3G, 4G and beyond), wireless data networks and Internet access, position location, navigation, roadway informatics, and wireless sensor networks. The necessity for low-cost and high-efficiency *system* implementations for these untethered communications capabilities has generated an explosion in the development of Radio Frequency Integrated Circuits (RFICs) [1]. These RFICs have generally been packaged together with VLSI digital signal processing (DSP) and microprocessor control chips on printed circuit boards (PCBs), or in advanced multichip modules (MCMs). However, on the immediate horizon are *mixed-signal* integrated circuits combining RF, analog, and digital functions on the same chip, rapidly approaching system-on-a-chip (SoC) implementations [2]. The development of such SoCs is motivated by lower packaging and handling costs, greater reliability, reduced size of the overall electronic system, reduced parasitic reactances, flexibility in impedance matching, and the ability to incorporate on-chip digital-domain filtering, frequency synthesis, etc.

Meanwhile, Silicon Germanium (SiGe) technology offers the unique ability to integrate both high-performance RF/microwave heterojunction bipolar transistors (HBTs) and high-speed/low-power complementary metal-oxide semiconductor (CMOS) transistors in the same IC environment. On the other hand, tremendous advances in submicron "RF" CMOS technologies have made single-chip system integration in CMOS-only a practical reality. In either case, there is a tremendous incentive to utilize Si-based technologies vs. other "exotics" in order to leverage the extensive existing fabrication and design infrastructure, and the corresponding economies-of-scale, afforded by silicon.

However, in conjunction with these technological advances, there has been a lack of skilled RF/analog/mixed-mode chip design engineers available to U.S. industry who could contribute to the development of such wireless SoCs. Therefore, our universities must develop new electrical engineering curriculum in the area of RF/analog integrated circuit design for wireless communications applications. Such curriculum can be significantly enhanced with the integration of "hands-on" design experience using industry-standard computer-aided design (CAD) tools and state-of-the-art integrated circuit technologies.

This paper will discuss the development of a new graduate-level Radio Frequency Integrated Circuit (RFIC) Design course at Virginia Tech. This course has been taught several times since 1999, evolving from a "special topics" course into a regularly scheduled course offering. In addition, the paper will describe the integration of a state-of-the-art commercial SiGe Bipolar/CMOS (BiCMOS) technology into the course through teaming with Motorola Semiconductor Products Sector. Student team designs from the course were successfully fabricated through Motorola SPS and delivered to Virginia Tech for follow-on testing.

II. **Course Structure and Content**:

RFIC Design (Virginia Tech course catalog number ECE 5220) is a graduate-level course offered by the Circuits and Electronics area focusing on the integrated circuit (IC) implementation of RF circuits for wireless communications applications. Prerequisite coursework includes senior/first-year-graduate-level (4000-level) coursework in RF Engineering or Microwave Engineering, as well as basic undergraduate-level background in electronic circuits and analog/digital communications. Previous exposure to VLSI CAD tools (e.g. through a standard digital VLSI design course) is desirable, but is currently not specifically required. Interestingly, enrollment in the course equally includes both EE students with stronger background in RF/microwave engineering and computer engineering students with stronger background in digital VLSI; this tends to create a culture of mixed-mode SoC design that is now a reality in the wireless communications IC industry.

Topics covered include: transceiver architectures for current wireless communications standards; active/passive device technologies for RFIC implementations; low noise amplifiers; mixers; frequency sources; and RFIC packaging and testing. These topics focus on the receive side of a communications transceiver, since there is another course at Virginia Tech that provides detailed coverage of power amplifier design (albeit not at the IC level). A percentage breakdown of the course coverage is provided in Table 1. Assigned textbooks for the course are B. Razavi's *RF Microelectronics* [3] and T.H. Lee's *The Design of CMOS Radio-Frequency Integrated Circuits* [4]. These texts are amply supplemented throughout the course by current and state-of-the-art conference and journal articles relevant to the above topics.

Table 1: RFIC Design course coverage breakdown.

Topic	% of Course
Review of basic concepts in RF Engineering (noise, nonlinearity, sensitivity, dynamic range, etc.)	15%
RFIC transceiver architectures (heterodyne, direct conversion, image rejection, etc.)	15%
Device technologies for RFIC (SiGe HBTs, RF CMOS, integrated passive components, varactors)	20%
Low Noise Amplifiers	10%
Mixers	10%
Voltage Controlled Oscillators and Phase Noise	15%
Phase-Locked-Loops and Synthesizers	10%
RFIC packaging and testing	5%

Homework assignments are front-loaded in the class schedule to exercise basic concepts in RF engineering, and device and system level issues. A midterm exam is subsequently scheduled (~9 weeks into a 16 week semester) to validate student knowledge of these concepts. In parallel with the homework assignments, a sequence of CAD tutorials are given in order to bring students up to speed on the CAD environment and provide them with some basic IC design experience, which is particularly important for students who have not had significant previous IC design experience (e.g. students coming from a traditional RF/microwave background). These tutorials will be discussed further below.

The course fundamentally involves "hands-on" circuit design at the IC level; state-of-the-art commercial RF/microwave CAD and layout software is used in conjunction with the course. The CAD environment will be discussed further below. The culmination of the course is a major course design project involving the design and full-custom layout of a functional block/component RFIC for wireless communications applications. The project guidelines are promulgated, and student design teams (typically 2-3 students per team) are assigned, ~10 weeks into the semester; the projects are due at the end of the semester. Typically no final exam is given, and the final design project report/presentation represents a significant portion of the course grade. In past years, the project assignment has focused on a specific functional block, such as a low-noise amplifier or a voltage controlled oscillator. More recently, the project assignment has been more open-ended. The project guidelines include suggestions for possible project topics, but students are free to propose variations on these topics, or even completely different topics, insofar as they are realistic given the technological and time limitations of the project. Details on some recent student projects are presented below.

III. Integration of State-of-the-Art Commercial SiGe IC Technology:

An outgrowth of the partnership between Motorola SPS and Virginia Tech in the RF/wireless microelectronics area has been access to their state-of-the-art HIP6WRF 0.18 μm SiGe:C BiCMOS technology [5] for student projects. This technology is based on a 0.18 μm low-power CMOS technology platform with dual gate oxide MOS device option and 5 layers of copper interconnect metallization. Low-threshold voltage CMOS, isolated NMOS, analog NPN BJTs, and high-quality passive components (thin-film resistors, metal-insulator-metal capacitors, etc.) are added for mixed-signal (analog/digital) and RF CMOS capabilities. In addition, the technology integrates high-frequency SiGe HBT devices (peak f_T = 50 GHz) for low-power, low-noise RF/microwave applications. Finally, the technology also offers a very thick electroplated Cu last metal layer for high-quality-factor RF passive components (monolithic inductors, transmission lines, etc.). Based on the availability of this technology for the RFIC Design course, the course content was enhanced to include specific coverage on SiGe HBTs, submicron RF CMOS, and copper interconnects/passives. Motorola provided full design kit support for this process for use in the RFIC Design course.

An important issue that had to be addressed was managing access to the proprietary information represented by the design kit and related process technology information. To address this, non-disclosure agreements (NDAs) were agreed on by both parties (Virginia Tech and Motorola SPS), and executed individually by each student and the responsible management personnel at Motorola. The NDAs restrict use of the design kit and related information for the purposes of the RFIC Design course for that semester.

IV. Computer-Aided Design:

A key aspect of the course was the use of industry-standard computer-aided design tools throughout the course. For RF simulation, the Cadence Spectre RF simulator was used [6]. In addition, the Momentum planar electromagnetic (EM) simulator, a component of the Agilent EESof Advanced Design System [7], was used for modeling of RF monolithic spiral inductors; incorporating EM simulation data into circuit simulations can yield more accurate simulation results. Circuit layout was performed using the Cadence Virtuoso software, and design-rule checks (DRC) and layout-versus-schematic checks are conducted on the circuit layouts to provide some assurance that the designs will be fabricated without fatal errors (however, these checks do not preclude design errors that might cause deviations or failures in the intended circuit operation).

Due to the complexity of the technology and the relative inexperience of some students in the area of IC design, a sequence of carefully designed CAD tutorials were provided to bring students up to speed on the use of the Cadence tools, and provide exposure to various aspects of the HIP6WRF technology. The topics of these tutorials are presented in Table 1. These tutorials are front-loaded in the course schedule such that they should be completed by the students prior to the assignment of the final course project.

Table 2: CAD Tutorials.

Tutorial	Topic
0	Getting started with Cadence
1	Creating Schematics and S-Parameter Simulations
2	Parametric Characterization of FET and HBT Devices
3	Layout and EM Simulation of Monolithic Inductors
4	Layout and Simulation of Current Mirrors

V. Recent Outcomes:

During Spring semester 2003, the RFIC Design course enrollment was 34 students. A Graduate Research Assistant from the principal author's research group was tasked to act as the graduate teaching assistant (GTA) and CAD resource for the course, and was instrumental in the preparation of the CAD tutorials described above.

For the course design project, the students were divided into 10 groups of 3 and 1 group of 4 by the instructor. Effort was made to balance the groups with regards to prior RF design experience and prior VLSI design experience to the maximum extent possible. Based on the timing of the project assignment in the course schedule, the focus of the project was on low-noise amplifier (LNA) design; however, the students had the freedom to propose different project topics if they so chose. Some groups elected to pursue RF mixer and VCO designs as part of their projects. The project topics selected by the students are summarized in Table 3.

The student teams designed and simulated their RFIC components in the HIP6WRF technology, and presented their design work at an end-of-semester design review. The design review was structured to be similar to those conducted in industry. Some designs were selected for fabrication on a subsequent HIP6WRF engineering mask run. Examples of selected designs included an X-Band LNA, UNII (5-6 GHz) Band VCOs, and LNAs with

temperature-independent biasing and Electrostatic Discharge (ESD) protection circuitry. The layouts for these selected designs were uploaded to a central class account during early summer and assembled together by the CAD GTA into an overall reticle design (Figure 1). In order to simplify the post-fabrication measurement requirements the RFIC layouts were configured to support on-wafer testing (GSG or GSSG probes), thereby eliminating chip dicing, packaging, and test board fabrication. Single-ended and differential calibration structures were added to the reticle to support the on-wafer measurement calibrations.

The selected RFIC course designs were successfully fabricated by Motorola and were delivered from the factory during November 2003. Testing of the fabricated designs is in progress. Figure 2 shows a photo of one of the class designs, a 5-6 GHz VCO, being measured using RF on-wafer probes. Also shown is a photo of one of the student design teams conducting measurements on their fabricated circuits.

Table 3: Spring 2003 Student Team Design Projects

Group #	Project Topic
1	Cascode vs. Transformer Feedback LNAs
2	2.4 GHz LNA for Bluetooth
3	Low-supply-voltage LNA
4	RF Front-End for 802.11x WLAN (included LNA, mixer and VCO)
5	Low-Power LNA for GPS with ESD Protection
6	WCDMA and GSM Dual-Band RF Front-End
7	2.4 GHz LNA for WLAN
8	2.4 GHz LNA Designs for Bluetooth
9	RF Low Noise Amplifier for Bluetooth
11	X-Band SiGe Low-Noise Amplifier
12	Low-Voltage Concurrent Dual-Band LNA
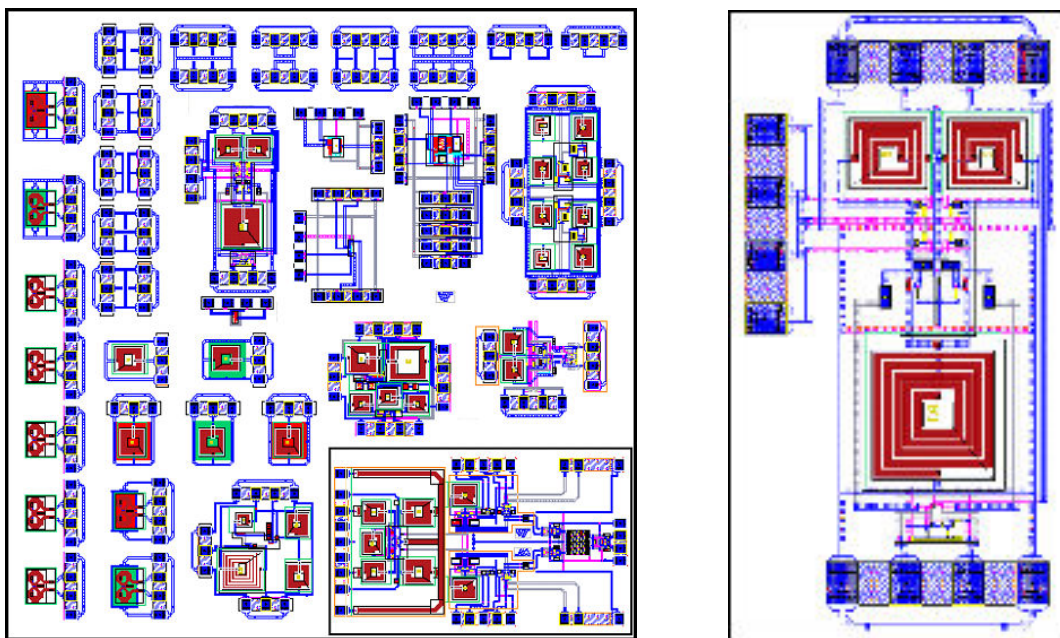
Figure 1. (Left) Layout of mask set reticle for fabrication through Motorola's HIP6WRF 0.18 μm SiGe BiCMOS process. (Right) Close-up of the layout of a 5-6 GHz voltage controlled oscillator design.
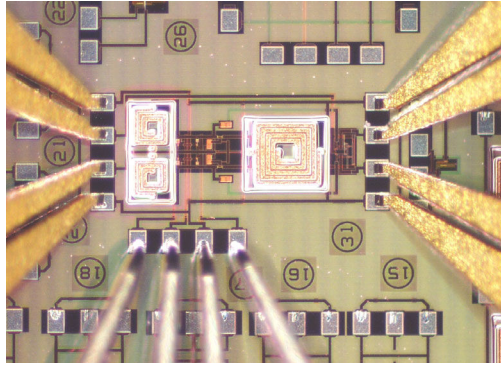
Figure 2. (Left) Student-team-designed Silicon Germanium 5-6 GHz Voltage Controlled Oscillator. The fabricated circuit is being measured using RF on-wafer probes. (Right) Student team conducting on-wafer measurements on their fabricated circuit.

Conclusions and Future Work:

This paper has discussed the development of a new graduate-level Radio Frequency Integrated Circuit (RFIC) Design course at Virginia Tech. Most recently, the course has been structured around Motorola's HIP6WRF SiGe BiCMOS technology for assignments and a major course design project. Selected student team designs from the course were successfully fabricated through Motorola SPS and delivered to Virginia Tech for follow-on testing; testing of these circuits is currently in progress.

For more information, check out the Spring 2003 ECE 5220 course website at: http://www.ee.vt.edu/~ece5220.

The long-term vision is a two-semester course sequence, adding a second semester follow-on laboratory course. The first semester (Spring semester) would essentially be the ECE 5220 lecture course described above. Student RFIC designs would be fabricated by the foundry during the summer break. The second semester (Fall semester) would be a follow-on laboratory course (1-2 hours) exposing students to wireless IC testing techniques including S-parameter, on-wafer and coaxial calibration, noise figure, phase noise, intermodulation distortion and spurious response, etc. measurements. Student teams will develop test plans for their fabricated ICs, and then execute the measurements in a state-of-the-art RF laboratory. At the end of the second term students will present their designs and measured results during a final project review. After completing the two-semester sequence, students will have experienced the RFIC design and fabrication process first hand, working in teams to develop IC designs and test plans, and will have acquired highly marketable skills for careers in RF/microwave engineering and IC design.

In addition a new senior/first-year-graduate-level (4000-level) Analog VLSI course is being developed by the primary author that will ultimately become a pre-requisite for the RFIC Design course along with the previously mentioned RF and Microwave Engineering courses. This would allow some fundamental analog IC concepts and CAD training to be moved out of the RFIC Design course into the prerequisite course, thereby freeing up valuable time in the schedule for additional RFIC-related topics such as RF power amplifiers. This new Analog VLSI course is scheduled to be offered for the first time in Fall 2004 in advance of the Spring 2005 offering of RFIC Design.

Ultimately, a team-based System-on-a-Chip project-based design course is envisioned. Such a course would bring together students with backgrounds in RF/analog IC design, digital VLSI design, test and verification, and digital signal processing/communications systems. It is expected that strong industry collaboration and mentoring would be a critical aspect of such a course.

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Biographical Information:

SANJAY RAMAN received the B.S.E.E. degree from Georgia Tech in 1987, and the M.S.E.E. and Ph.D. degrees from the University of Michigan, Ann Arbor, in 1993 and 1997, respectively. He joined the faculty of the Bradley Department of Electrical and Computer Engineering at Virginia Tech, Blacksburg, VA, in 1998, where he is currently an Assistant Professor and Director of the Wireless Microsystems Laboratory.

ADAM KLEIN received the B.S.E.E. degree from Cal Poly Pomona in 2001, and will receive the M.S.E.E. degree from Virginia Tech in 2004. In the summer of 2002, he interned with the Wireless Broadband Systems Group at Motorola SPS. He joined the Wireless Microsystems Laboratory at Virginia Tech in 2002 where his research has involved RF VCO design in SiGe and Si CMOS technologies. He was also the GTA for the RFIC design course during Spring 2003.

RICHARD SVITEK received the B.S.E.E. degree from The University of Pittsburgh in 1998 and the M.S.E.E. degree from Virginia Tech in 2002. He is currently a Ph.D. candidate in Electrical Engineering at Virginia Tech as a research assistant in the Wireless Microsystems Laboratory. His research involves the development of novel RFIC direct conversion and low-IF receivers and related components in SiGe BiCMOS technology.

CHRISTOPHER MAGNELLA is a 1984 graduate of Virginia Tech (Materials Engineering). He has 19 years of semiconductor process engineering, engineering management and manufacturing management experience working at Analog Devices, Harris Corporation and, for the last 14 years, Motorola. Chris is currently Chief of Staff for the 32 Bit Embedded Controller division in Austin, Texas.

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ERIC MAASS received the B.S. degree from Univ. of Maryland in 1975, and the MS in Chemical and Biomedical Eng. from Arizona State Univ. in 1982. He joined Motorola in 1979, and has held a variety of technical/managerial roles including device engineering manager, operations manager, design/systems manager, and director of technology strategy. He is currently leading efforts to apply Six Sigma methodology to new product development.