An Unsophisticated Printed Circuit Board Fabrication Process Requiring Only a Laser Printer and Copper Etchant

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Abstract

A low-cost method of fabricating a Printed Circuit Board (PCB) is presented. The process is favorable over conventional PCB fabrication due to fewer processing steps and lower capital investment. A laser printer is used to print a circuit layout onto ink-jet paper or a commercial product (i.e. PnP-Blue from Technics, Inc.). The image is then transferred to a copper clad board using a standard household clothes iron. The transferred toner acts as an etch resist in a Ferric Chloride ($FeCl_3$) bath. Using this method, it is possible to fabricate PCBs with state-of-the art feature sizes as small as 4 mils using a 300 dpi laser printer. A higher resolution printer is expected to give finer resolutions. Tradeoffs between the ink-jet paper and the PnP-Blue paper will be analyzed and discussed. This approach has been used for graduate-level courses including a VHDL class project to implement an ALU using a 44-pin CPLD and a microwave class project to implement a microstrip matching networks using a cellular band power transistor.

I. INTRODUCTION

The current Printed Circuit Board (PCB) technology routinely prints trace widths of 6 mils as found in a typical four-layer PCB used in desktop PC motherboard [1]. The equipment to produce such PCBs in high volumes can cost well into the hundreds of thousands of dollars, which is prohibitive for many universities and potential start-up companies. Even when less than state-of-the-art equipment is available, the process itself may limit its usefulness in a classroom setting as it requires the following steps:

1. Mask generation
2. Resist deposition
3. Resist exposure using ultraviolet lamps
4. Resist development
5. Copper etching bath

6 Resist removal bath

If a laboratory is not already in place to perform these steps, the cost to do so may not be justified for a single course. Another factor is that the necessary chemicals are toxic, especially the resist stripper, and care must be taken in using and disposing of them. The purpose of this work is to make creating a single layer PCB simple, cost effective, safer and more environmentally friendly by replacing the above six step process with a simple, inexpensive two step process:

1. Apply Laser printer generated mask to a copper board
2. Etch the copper board directly in a standard etch bath, i.e. $FeCl_3$.

This simple, extremely cost-effective process can be easily achieved at any university even if the procedure is only used for a single course. This process has been used by a class of fifty electrical engineering and computer science students to demonstrate a hardware project utilizing a single layer PCB populated with standard components including a 44-pin Complex Programmable Logic Device (CPLD).

II. PROCESS DESIGN

A. Overview

Two, low-cost, low-tech methods of creating a single layer PCB were tested. Both methods were similar in that a standard laser printer was used to print a mirrored positive image of the circuit traces onto a transfer sheet. This image was then transferred onto the copper board. This image acts as an etch resist in the copper etch bath.

The first approach used a commercially available product called PnP-Blue manufactured by Technics and purchased from ALL Electronics (1-800-826-5432). The PnP-Blue is an 8.5 by 11 inch sheet resembling an overhead transparency with a blue powder loosely adhered to one side. The second approach tested used standard ink jet paper in place of the PnP-Blue. The ink jet paper was chosen for its smooth surface allowing an easier transfer of the toner to the board as well as much lower cost. A test pattern was designed to evaluate the repeatability and effectiveness of the process. The test pattern consisted of a series of “L” shaped lines having line widths from 1 mil to 50 mils with large gaps between the lines to determine the accuracy of single trace lines. Another evaluation structure on the test pattern consisted of a series of straight lines for a spacing test. The drawn lines had a width of 12 mils to look at how close adjacent lines could be placed. The spacing between lines varied from 1 mil to 50 mils. The last evaluation structure on the test pattern contained typical PCB trace patterns, such as chip surface mount solder pads and through-hole pads. In addition traces were routed in between the pad traces to acquire some understanding of worst case routing possibilities. The PnP-Blue paper image of the test pattern is shown in Figure 1.

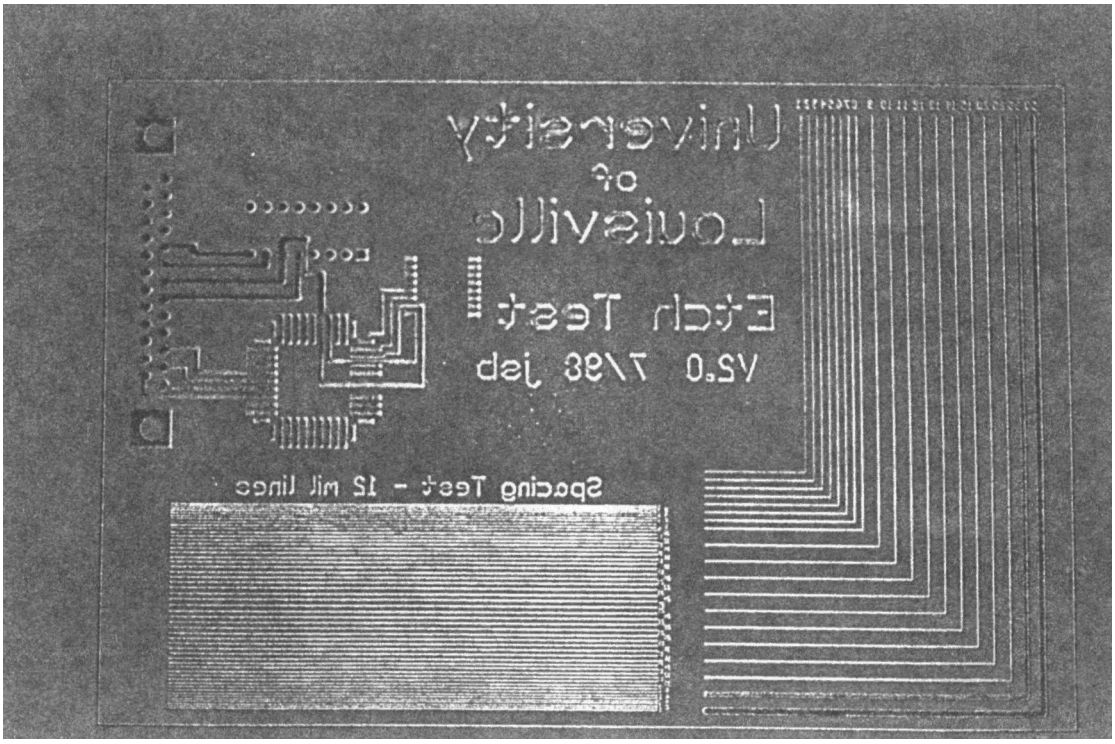

Fig. 1. PnP-Blue plotter paper test pattern mask after being fed through the laser printer.

B. Procedure

Design the circuit layout using the software of your choice. There are many CAD/CAM PCB programs available for laying out the circuit. A program used by the majority of the class was EasyTrax, a freeware program available at [http://www.omnigraph.com/software.html]. A requirement of the layout software for this process is that it be able to print a mirror image of the circuit layout.

Once your layout is complete, print the circuit from a laser printer on standard printer paper to verify that all components will fit as designed and that the entire circuit properly fits the printed circuit board being used. To do this, put the components on the printout and ensure that all pins can simultaneously make contact. Once you are satisfied that the layout is correct, you are ready to transfer the design onto the copper clad board.

First, clean the copper board by scrubbing the surface with a wet ScotchBrite pad or steelwool. This will remove surface oxidation and oil for better adhesion during the transfer process. Then print the mirror image of your design onto the PnP-Blue (powder side) or ink jet paper. You want the printed image to be as dark as possible without causing smudges on non-trace areas. After printing, cut the image out of the transfer sheet leaving a minimum of 1/4" around the circuit pattern.

You will use a standard household clothes iron to transfer the image from the transfer paper to your cleaned circuit board. The temperature setting is dependent upon the type of toner used in your printer. Usually a temperature around 200-225^{o} F will work best. A good place to start is with a setting in the lower region of the "Steam" settings or about 2/3 of the iron's maximum setting. This should be a dry process so do not add water to the iron.

Begin by placing your circuit board, copper side up, onto a piece of wood or similar heat insulating material. A short stack of paper (10 sheets or so) works well. You want a firm surface which will not get too hot during ironing. Next, place the transfer sheet with the image facing down onto the circuit board and begin ironing, applying the heat in a circular motion. Begin by concentrating on one corner until it adheres to the copper surface. This will help to hold the paper in place while working on other areas. You will begin to see the image of your design through the back of the transfer sheet as you continue to iron. Use this as a guide to ensure that you are heating the entire surface evenly, paying special attention to the outer edges of the board. The entire process could take as little as 45 to 100 seconds but it is recommended that you continue to iron for at least 5 minutes. In some cases this improves the chances of getting a good transfer at the cost of lower resolution.

After ironing, allow the board and paper to completely cool (10 to 15 minutes). After cooling, carefully remove the film by pulling back the corner 180 degrees and "roll" the film off the board. You are now ready to etch the board.

Before etching the board, inspect the board for shorts and opens. Shorted traces are most easily corrected at this stage with a utility knife. Voids (opens) can be corrected by placing scotch tape over the void. The tape will be an effective etch resist.

The copper not masked by the transferred image will be removed by etching in a heated Ferric Chloride ($FeCl_3$) solution. Before using the Ferric Chloride solution it is important to fully understand the associated health hazards and safety precautions. Read the Material Safety Data Sheet (MSDS) and enforcing a few simple rules will help to insure the safety of the students.

- Handle under a fume hood whenever possible.
- Wear rubber gloves and eye protection whenever handling solution.

- Ferric Chloride will stain anything that it contacts. You may want to wear an apron or lab coat to protect clothing.

Start by pouring about an inch of Ferric Chloride into a Pyrex tray. Place the tray on the hot plate and bring the solution to the optimal temperature of 40^{o}C. DO NOT exceed this temperature or excessive fumes may occur. Once you have reached the desired temperature, carefully place the board to be etched into the tray with the copper side of the board facing up. Since the solution will etch substantially faster when agitated you will need to rock the tray from side to side throughout the process.

The rate at which the board etches is dependent on many factors including the rate of agitation, temperature and the amount of metal in the solution. Therefore, it is impossible to determine an exact etch time. You should expect the process to take from 20 to 50 minutes. When the board is mostly etched, there may be a few spots with copper remaining. Use a Q-Tip to rub additional Ferric Chloride on these areas. At this point the rubbing action should remove any remaining copper rather quickly.

Once the etching is complete, rinse the board under running water for several minutes to clean the copper board. Inspect the copper traces for opens or shorts. Some shorts can be repaired using a utility knife while opens can be repaired using jumper wires. The traces will appear dark since they are still covered by the toner and etch resist from the PnP-Blue paper. When using plotter or ink-jet paper, the toner can easily be removed with acetone or sandpaper. However, acetone does not remove the PnPBlue paper residue. You can use a fine grit sandpaper or steelwool to remove this residue. A picture of the completed test pattern board after cleaning up the copper is shown in Fig. 2.

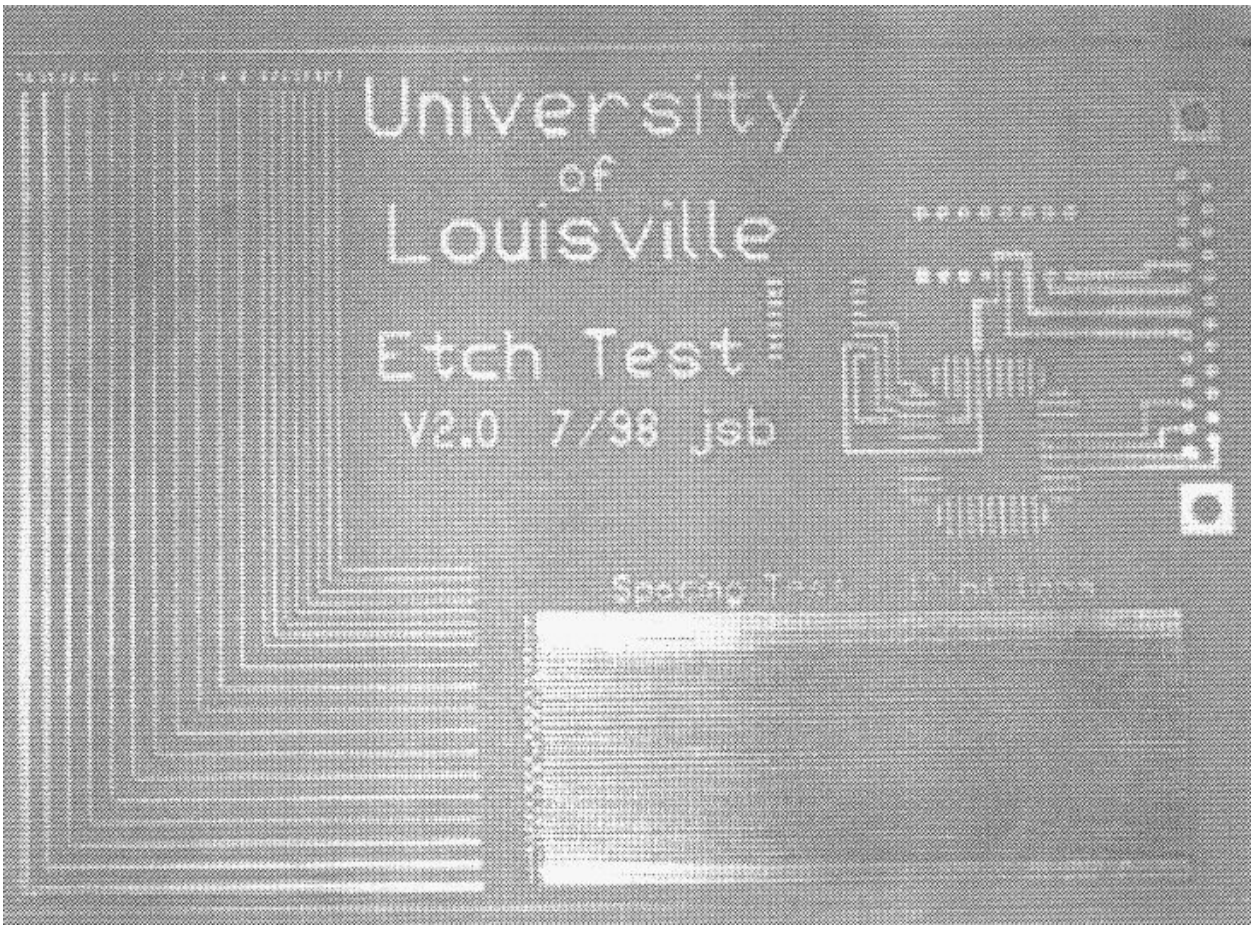

Fig. 2. Test pattern PCB after copper etching and resist cleanup.

III. DEMONSTRATION VEHICLES

A. VHDL Based ALU Project

A key benefit of this PCB process in an academic environment is in the affordability of a hardware implementation of a circuit design that would otherwise be accessible to the student only through computer simulation. The process was tested in a hardware project assigned to University of Louisville's Electrical Engineering and Computer Science students enrolled in a graduate level VHDL and programmable logic design course during the summer term of 1998. The course presented students with a hardware-level description of CPLDs and FPGAs and proceeded into the use of VHDL software to program these devices. The culmination of the course was a hardware project based on the design of a 4-bit microprocessor using VHDL. The students were tasked with synthesizing the ALU portion of the microprocessor using a behavioral level VHDL description of the circuit. The project then required the students to

implement and verify the design in hardware by utilizing the board fabrication process and a 44-pin surface mount PLCC CPLD.

In order to make the project more manageable in the constraints of available time and hardware, the design was reduced to a 3-bit ALU without loss of instructive benefit. The inputs to the ALU were two 3-bit binary words, R and S, and a 3-bit binary ALU instruction selection. Table 1 lists the ALU instruction set. The output was to be displayed on two seven-segment LEDs in decimal form.

Table 1: Instruction set for the 3-bit ALU design.

Selection Word	Function
000	S – R
001	R – S
010	R + S
011	R AND S
100	R OR S
101	R XOR S
110	(NOTR) AND S
111	(NOT S) AND R

The text used for the course [2], included WARP, a VHDL compiler written by Cypress Semiconductor that runs on a PC. Capabilities include compilation, simulation, timing analysis, JEDEC file generation. and placing and routing. A 44-pin Cypress CY7C372I CPLD was chosen to implement the ALU. It has 64 macrocells with the ability to create up 6192 product terms. Figure 3 shows a schematic of the hardware that was populated on the board.

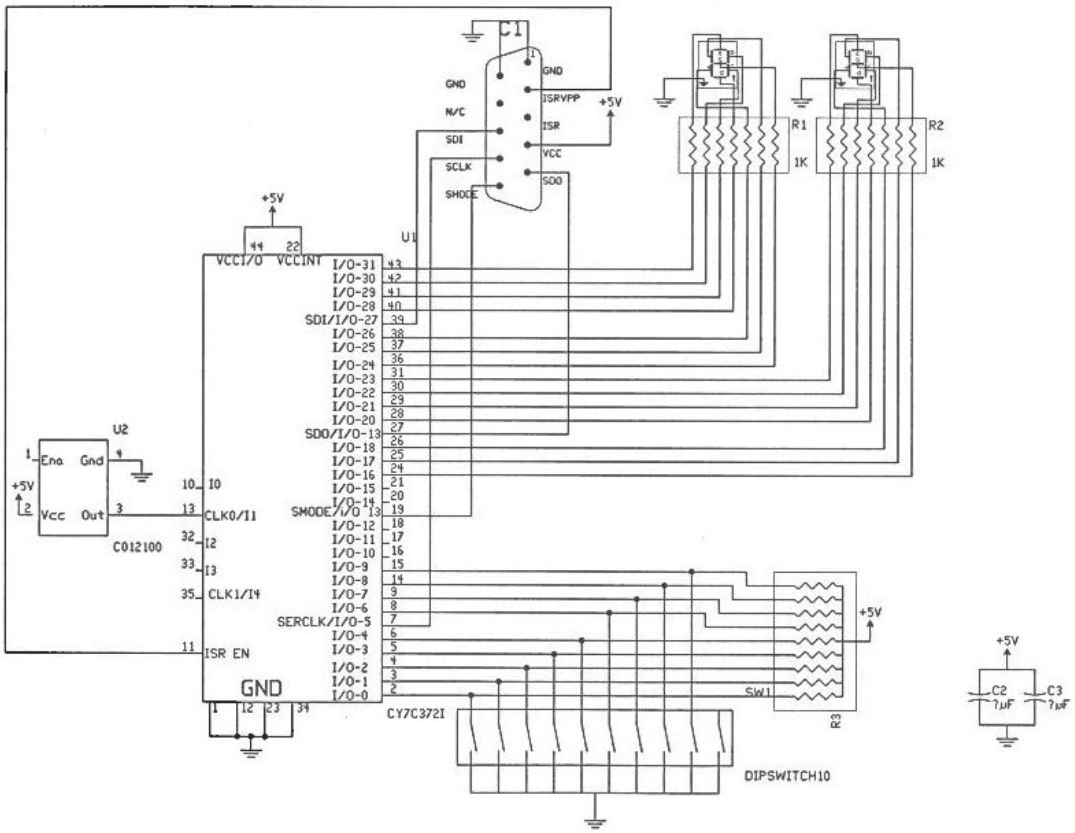

Figure 3. Schematic of the CPLD-ALU demonstration PCB.

Nine DIP switches were used to generate the three 3-bit input words: R, S, and the instruction selection. A bank of nine 15kΩ resistors was used to pull the inputs to the CPLD high when the DIP switches are open. The CPLD outputs, capable of driving the LED segments directly, were connected through 680Ω resistors to the LEDs. Additionally, a 10-pin header was utilized to connect the In-System-Reprogrammable (ISR) programming cable from the PC to the board.

The ALU was coded in VHDL using WARP software and simulated in NOVA, the simulation package accompanying WARP. Successful compilation of the VHDL code resulted in the generation of a JEDEC file which was then utilized by ISR programming software. To program the CPLD, the ISR programming cable was connected from the parallel port of the PC to the programming header on the board, and the ISR software was invoked to implement the design based upon the JEDEC file.

The project provided the students with a "hands-on" design experience that incorporated layout design, board fabrication, component selection, board soldering, VHDL design, debugging and testing. Student groups of two were required to individually design and fabricate a single layer printed circuit board to meet project specification. The teaming arrangement is also important to help prepare the students for teamwork environment of industry. Components were then

soldered onto the board in a surface mount fashion, eliminating the need for drilling holes. Some students choose to use 100 mil pitch through-hole components to make the soldering easier by avoiding the standard 50 mil pitch of surface mount components. The board was then tested for correct operation using a very simple VHDL test program to turn on the LEDs when a DIP switch was activated. Successively, the 3-bit ALU was written and programmed into the CPLD. A demonstration of the correct operation was required. A picture of the final fabricated and tested board is shown in Fig. 4

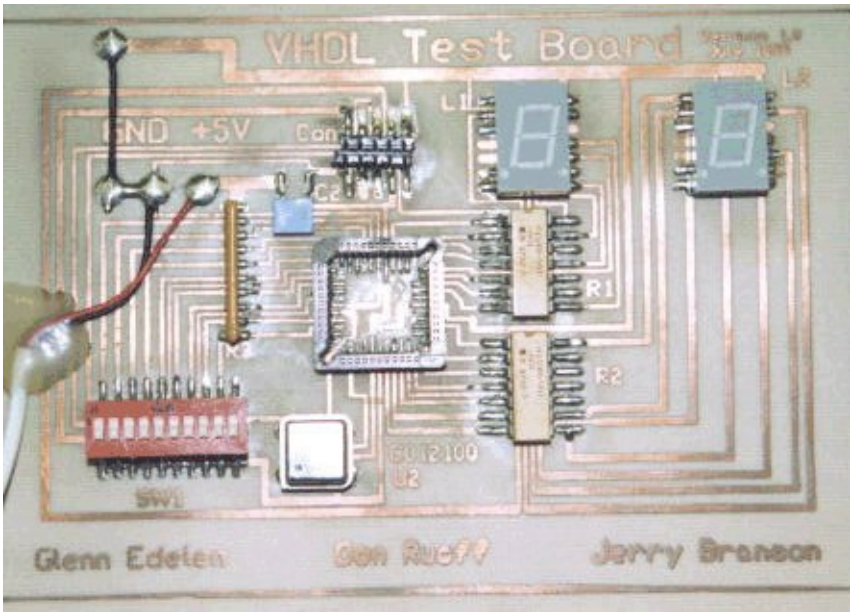

Fig. 4. Picture of the final ALU test board without the CPLD in the socket.

B. Cellular Band Power Amplifier with Microstrip Matching Project

The academic environment benefit of affordability and student accessibility is extended to practical applications with its high repeatability. Since this process yields predictable, consistent results, it can be used for processes which require specific trace widths and shapes. The process was tested in a hardware project assigned to University of Louisville's Electrical Engineering students enrolled in a graduate level Microwave Engineering course during the fall term of 1998. The course presented students with a hardware-level description of microwave fundamentals and proceeded into the use of the Smith Chart and Microwave Design software to design microwave microstrip matching networks. The culmination of the course was a hardware project based on the design of cellular band power amplifier. The students were tasked with designing a power amplifier for maximum gain in the 950 MHz Cellular phone band including microstrip matching networks. The project then required the students to implement and verify the design in hardware by utilizing the board fabrication process and a microwave power transistor.

In order to make the project more manageable in the constraints of available time and hardware, the design was reduced to matching only - the biasing would be done off board using standard bias T's.

The software Libra was used during the course. The majority of the students used a hybrid design technique to design the matching networks using a Smith chart and hand calculations to obtain a unilateral approximate design which minimized S11 and S22. Libra was then utilized to check the design and refine the microstrip dimensions utilizing bilateral design techniques including the use of S12 and S21. Figure 5 shows a schematic of the design that was constructed on the board.

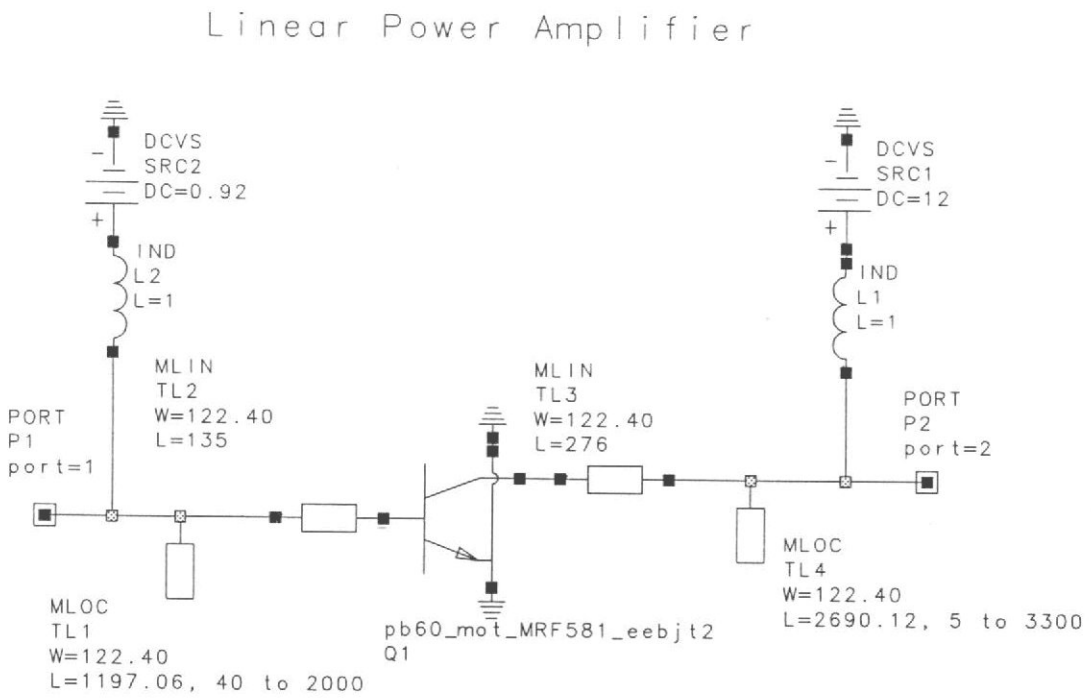

Figure 5. Schematic of Cellular Band Power Amplifier Design.

The project provided the students with a "hands-on" RF experience that incorporated DC circuit analysis, RF circuit and layout design, board fabrication, and RF measurement techniques. Student groups of two were required to individually design and fabricate a double layer printed circuit board to meet project specification. The teaming arrangement is also important to help prepare the students for teamwork environment of industry. The microwave transistor and connectors were then soldered onto the board. Unlike the VHDL project, it was necessary to pay close attention to soldering techniques, ensuring good, low inductance soldering joints. The board was then tested for correct operation using a simple test setup which measured the gain at different frequencies and power levels. A contest was held for the maximum gain and the course

grade was based partially upon the gain achieved. A picture of the final fabricated and tested board is shown in Fig. 6.

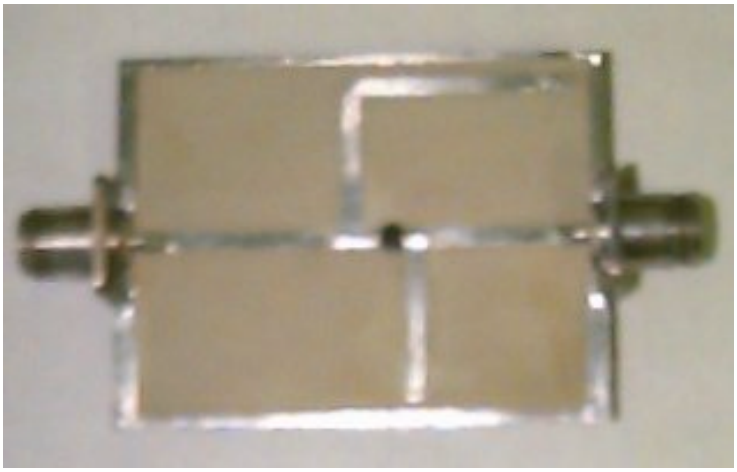

Fig. 6. Picture of the final Cellular Band Power Amplifier.

IV. DISCUSSION

A. Classroom Results

Groups of two or three students worked independently on the design projects, and while their board layout and component selection varied, every group successfully completed the projects. Various layout editors were used with similar success. The 44-pin CPLD provided a reasonably challenging requirement which tested both the design competence of the students and the capabilities of the board fabrication process. The Microwave transistor provided a reasonably challenging requirement which additionally tested the students' abilities to provide consistent high quality, low inductance solder joints and conductance paths. Students were responsible for ordering their own parts and allowed to expand upon the project requirements yielding a diversity of boards.

The VHDL course consisted of both Electrical Engineering and Computer Science students, while the microwave course consisted of Electrical Engineering students. Valuable "real world" design experience was acquired from the VHDL synthesis, board layout and selection of parts to meet the specifications of the project. Also, competence in the PCB fabrication process, soldering of the components to the board, and board testing was achieved, especially important for the microwave project. VHDL code had to be optimally written within the limitations of the CPLD. Students gained the experience of in-system programming of a CPLD.

B. Tradeoffs Between PnP-Blue and Plotter Paper

The above process works when using both PnP-Blue and standard ink jet paper. Each method has advantages and disadvantages over the other.

The PnP-Blue paper provided for an easier transfer of the image to the copper board. The blue powder acts as a release allowing the toner to transfer more easily. Using this method, 75% of the boards transferred correctly on the first attempt. When using the ink jet paper, a good transfer was achieved 33% of the time.

A minor advantage was the shorter ironing times realized when using the PnP paper. The transfer could be completed in less then 100 seconds using this method, while ink jet paper required ironing times closer to 5 minutes.

The advantages of the ink jet paper are reduced cost, wider availability, and smaller feature sizes. While the PnP paper cost $2.39 per page, the ink jet paper cost approximately 10 cents per page. Even considering that several attempts may have to be made to achieve a good transfer, there is still a considerable cost savings. Also, the ink jet paper is more readily available from local sources. Smaller feature sizes were achieved with the ink jet paper. PnP-Blue yielded traces of 15 mils, while ink jet paper yielded traces of 4 mils using a 300 dpi laser printer. The reason for this is that the blue powder tended to spread out during the ironing process.

V. CONCLUSIONS

This PCB fabrication process presented above has the following advantages over traditional methods:

- Fewer wet processes.
- Lower capital and production costs.
- Faster turnaround.
- Simple process available to the student.

The process combines affordability and quality with state-of-the art trace widths and spacings as small as 4 mils using only a 300 dpi laser printer. This results in approximately 1.2 printed dots per 4 mil line. It is hypothesized that a 1200 dpi laser printer should be able to print reproducible lines down to widths of 1 mil. This single layer approach can also be applied to two-sided boards in a straightforward manner. The most critical step using a two-sided board is the alignment of the masks prior to iron transfer. Hence for a reasonable yield it is imperative to give excessive tolerance to the through-hole dimensions, so alignment becomes less critical.

This PCB process has a wide range of applications to a variety of students. This simplistic PCB fabrication process provides students with a fast, easy, and inexpensive source of PCBs that is intrinsically safer for the students to handle over previous processes. Furthermore this process is much more environmentally friendly by all-together avoiding toxic resist strippers. The process is extremely useful for courses in which a hardware project is required. For example, this process

allowed students learning VHDL to actually see their software design of a 3-bit ALU come to life using this PCB process with a programmable logic device.

REFERENCES:

[1] R. Marrs, “Trends in IC Packaging and Advanced Assembly”, Electronic Packaging and Production, pp. 26 – 32, July 1998.

[2] K. Skahill, “VHDL for Programmable Logic”, Addison-Wesley, New York, 1996.

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