DARPA's Digital System Design Curriculum and Peer-Reviewed Educational Infrastructure

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Abstract

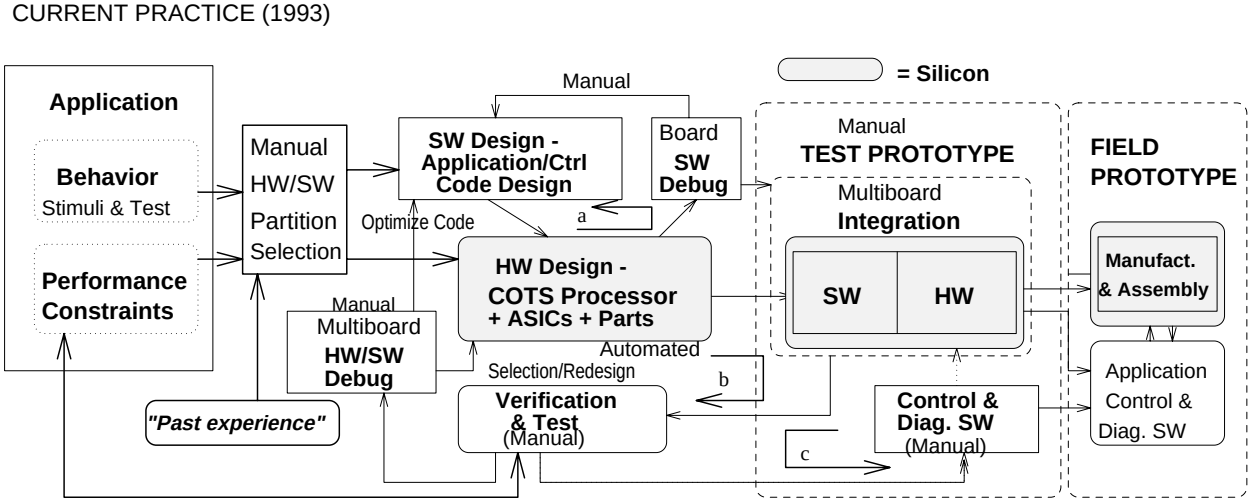
As part of DARPA's $150M Rapid Prototyping of Application Specific Signal Processors (RASSP) program, the RASSP Education & Facilitation (RASSP E&F) team consisting of SCRA, Georgia Institute of Technology, University of Virginia, University of Cincinnati, Raytheon, and Arthur D. Little has developed a new digital system design curriculum and supporting course infrastructure in the form of an electronic archive of instructional material – course modules, labs, projects, and interactive educational CD-ROMs. Included in this electronic archive or digital library are over 200 hours of instructional material suitable for immediate insertion at the undergraduate and graduate levels. To date, over 80 educational institutions have obtained educational material developed by the RASSP E&F team. In this paper, we present the technical goals and rationale, including an Educational Maturity Model (EMM), motivating our efforts. Additional details are available on our WWW server: <http://rassp.scra.org>.

1. Introduction

The Department of Defense Advanced Research Projects Agency (DARPA) sponsored Rapid Prototyping of Application-Specific Signal Processors (RASSP) program is targeted towards the design, prototyping (from concept to product), and procurement, of large embedded digital systems. Examples of systems of interest range from efficiently packaged single-board embedded systems (as found in high-performance workstations using MCMs) to large multi-chassis radar signal processor systems which typically have performance requirements ranging between 20-1000 BFLOPs (billions of floating operations per second) of computational intensity at pixel rates of 10 MHz, within the form constraints of size, weight, and power of 0.05-1.5m^3, 40-500 Kg, and 1-10 KW, respectively. Boards represent sub-systems, while multi-board configurations can represent complete systems, and involve hardware fabrication, assembly, and integration with application, control and diagnostic software. Clearly, the RASSP program is of strategic importance to industrial and military competitiveness [6].

RASSP promotes a new design methodology for digital systems prototyping that differs from current design practice as taught in our universities and practiced in the past. Figure 1 represents a high-level depiction of current design practice (circa 1993) for large embedded systems with a data processing section and its associated microcontrol. The design process flow diagram starts with a definition of the requirements for the embedded application (e.g., algorithmic requirements). The behavior of the application (e.g., a STAP/SAR radar signal processor

system) is then specified in an executable form (a VHDL/Ada, or a C/Matlab program) together with stimuli and test benches. In addition, the system has certain form-fit characteristics and constraints that must be met by the prototype (representative values being given in the preceding paragraphs).



Shaded areas represent hardware assembly, fabrication or manufacture.

Figure 1. Current Practice Model of System Design

After an appraisal of the embedded application characteristics is completed, a partitioning of the application into hardware (HW) and software (SW) is carried out. This is typically carried out manually by an experienced hardware system designer in an often *ad hoc* fashion. Common-off-the-shelf (COTS) components, FPGA and ASICs are then allocated and HW partitions are mapped onto these components. COTS components such as processors and memories are chosen as targets for the mapping of SW partitions. Initial estimates of resources are then determined based on the allocations that have been performed. The application is then partitioned into subsystems (boards) so that each of these boards executes a portion (in SW or HW) of the algorithm. This prototype system will then be tested and benchmarked to verify that all of the specifications and requirements are meet.

Since software (SW) cannot execute without target hardware, application and control software can only be tested and debugged after the hardware fabrication (assembly) and test is completed (which can take 2 – 4 months per board). After the hardware is fabricated, application and control code is debugged in an iterative design cycle as illustrated in Figure 1. After successful design and test of the board-level HW/SW subsystem, the multi-board system is integrated manually, wherein the software and the hardware are merged and tested via diagnostic software and input from the application (stimuli and test). This integration is done manually and may involve silicon fabrication, manufacture and assembly/test, and is iteratively refined until an acceptable prototype is produced. The development of an acceptable prototype often involves delays totaling 3 – 4 years, at the cost of 20 – 30 man-years because the three software design loops **a**, **b**, and **c** shown in Figure 1 all include hardware fabrication.

In one representative operational (late 1992) STAP radar signal processor system, the final HW count was about 150 boards incorporating a total of about 25,000 LSI/COTS components including an ASIC front-end filter and a 64-processor TMS320C30-based processing engine. The final SW count in *lines of source code* (LOSC) was 5K LOSC for the DSP/radar signal processor application, 30K LOSC for control, 60K LOSC for diagnostics, and 25K LOSC for functional and performance verification, representing a ratio of more than 20:1 in diagnostic and control code to DSP application code.

Only high volume, low cost, consumer products rely on hardware-only solutions It may be observed that very little software design is covered in current digital design curricula even though more than 80% of current functionality is implemented in software.

The RASSP program has developed a top-down, reuse-based virtual prototyping design methodology that extends and integrates a number of advanced technologies to dramatically reduce the time required to go from concept to prototype for embedded systems. These technologies include model year architectures, executable specifications and requirements, cost modeling for design, HW/SW codesign, virtual HW/SW integration and test, software design and test, performance modeling, distributed collaborative design, VHDL-based system modeling, and enterprise integration. These technologies cover all aspects of the system design process. The current digital system design curriculum in the universities covers only a small subset of these technologies (mainly in the area of chip design and logic synthesis). While these technologies are based upon research done within universities that has been perfected by industry, it is hoped that these technologies would be included in the university classrooms in a timely manner. This transfer has been slower than desirable. In this paper, we will attempt to investigate why this is the case, and how this problem is being addressed by the industry, academia and the government as part of the RASSP program through the RASSP Education & Facilitation (RASSP E&F) effort. The RASSP E&F program is a dedicated effort focused on transferring the technology developed by the $150M RASSP program into academia and industry.

2. A Need for Change

Science is generally based on experimental methods that allow the formulation of general theoretical constructs. Applied sciences focus scientific theory to purposeful activity. Technology and engineering, on the other hand, put applied science to work efficiently in a process context. While science seeks basic understanding, technology and engineering are primarily goal-oriented activities in response to societal needs [4,5].

Technical and engineering knowledge can take three forms. *Descriptive* knowledge describes things as they are, usually rules, general concepts, and principles in a narrative manner. *Prescriptive* knowledge is the technical know-how gained from repeated application of descriptive knowledge, and can be captured and transferred via demonstrations and homework exercises. Finally, *tacit* knowledge is implicit. This encompasses “tricks of the trade,” including protected and competitively sensitive knowledge. Shop floor and “skunk works” type innovations are difficult to capture, and tacit knowledge can only be learned by doing. Thus “hands-on” or *proximal* learning methodologies are most suitable for transferring tacit technological knowledge.

Given the above definitions, universities have been the incubators for developments in science and applied sciences, while the industry has been the primary source of technological knowledge. This technological knowledge when transmitted into the university curriculum results in further developments in the engineering and science arenas. In return, the academic community provides the industry with skilled personnel and innovative new ideas that it needs to succeed. This natural synergistic relationship and knowledge transfer between the universities and the industry has resulted in the enormous technological progress witnessed in this century. While this equilibrium has been carefully maintained until the '80s, many recent developments have had a disruptive influence, resulting in the current climate where the industry blames the educational community for not meeting its immediate needs in results or trained personnel, while the academia, in turn, blames the industry for focusing on short term profits as opposed to long term strategic technical goals [5]. Resources for new research in both arenas have been severely cut (e.g., dismantling of Bell Laboratories, and reduction in industry-sponsored basic research on university campuses), further compounding the problem. Is there a sudden disillusionment with an educational system that has served us so well for over three decades, or are some industry and university players crying wolf? The National Academy of Engineering also recognizes this problem and argues for an educational system that is relevant to the needs of the community [3].

If one accepts that there is some truth to this claim, the underlying causes for this disillusionment are many. First, there is an enormous amount of technical knowledge that has been generated in the past few years. For instance, the IEEE published only a handful of journals in the '60s, but currently publishes several hundred journals each month. This explosive growth in knowledge with only small increases in faculty resources when combined with a relatively constant number of credit hours required for graduation, has, in many cases, resulted in a natural selection of mature technologies for inclusion in the classroom versus state-of-the-art technologies. The lack of a consistent evaluation mechanism has also tended to make the choice of college courses (to introduce, or to phase out) subjective at best. Thus, it has been difficult to define a curriculum that is relevant to the diverse needs of the industrial community.

Second, the lifetime of technological developments has dropped from decades in the '60s, to a few years (in some cases to a few months) in the '90s. This increasing rate of technological change highlights the problems that universities currently have in assimilating new technologies into their curriculum.

In addition, many developments in the industry, by its prescriptive and tacit nature, seldom find their way into publications that can be used to transfer technology into the university curriculum. What is needed appears to be a communication gateway that captures relevant industrial knowledge in a form that can be quickly introduced into university curricula by faculty who would otherwise have little experience in these new technologies themselves. In addition, a path that conveys recent university research results in a form that facilitates learning and therefore technology transfer from academia to industry is also needed. This paper presents an approach to meeting these challenges that has been developed by the DARPA funded RASSP E&F program.

3. The RASSP E&F Program

The $150M RASSP program has developed several vital and strategic technologies in the area of complex electronic system design. It was felt that the government and industry would greatly benefit from the rapid proliferation of this technology. To achieve this result, DARPA determined that it could not risk relying on conventional diffusive means. It was felt that a focused effort was necessary. The RASSP Education & Facilitation (E&F) program is a ground-breaking effort explicitly funded to transfer technology from the RASSP program to the university and industrial communities.

The RASSP E&F goals may be summarized as follows:

1. Propose a relevant curriculum in system-level design and create a high quality base of educational material based on the results of the RASSP program to support this curriculum;
2. Propose and implement a model for technology transfer commensurate with the needs of industry and academia;
3. Utilize modern technologies, such as distributed collaboration and the WWW, to provide the necessary infrastructure to support technology transfer.

3.1 Bloom's Learning Taxonomy

In facilitating the accomplishment of the RASSP E&F goals, we found Bloom's taxonomy [2] very useful in the development of a novel Educational Maturity Model (EMM). Bloom classified learning in the classroom into the following set of levels:

- *Knowledge*: Student learns terminology, facts, and definitions, including benefits of applying the technology under study;
- *Comprehension*: Student can make use of ideas and material without seeing their full implication. Extrapolation to new situations is possible in limited context;
- *Application*: Student can apply knowledge to practical cases through the use of tools;
- *Analysis*: Student can break down the components of a system, and can identify hierarchies and relationship between elements. Organizational structures and assumptions (unstated) can be recognized;
- *Synthesis*: Student is able to synthesize a system from the start, using decomposition methods or otherwise. This includes the ability to produce a plan to design and implement the system and a mechanism to verify that the plan works and will achieve the objectives;
- *Evaluation*: Student can evaluate, compare, critique, and judge various alternative solutions and improve upon a solution;

3.2 Educational Maturity Model (EMM)

Derived from Bloom's taxonomy, we propose the so-called Educational Maturity Model (EMM). This model allows us to classify the levels of maturity of educational material.

1. *Basic* – This level of material supports knowledge and comprehension abilities on the part of the student.
2. *Applicative* – This level indicates that educational material facilitates usage of tools and application of knowledge to practical problems in limited context. Knowledge is primarily narrative.
3. *Deductive* – Supports learning of analytical aspects of technology, and the capability to apply general principles to specific cases. Prescriptive aspects of the knowledge are transferred at this level.
4. *Productive* – This level supports the synthesis and evaluative aspects of learning and is the most advanced level. Included in this level are the tacit aspects of a technology.

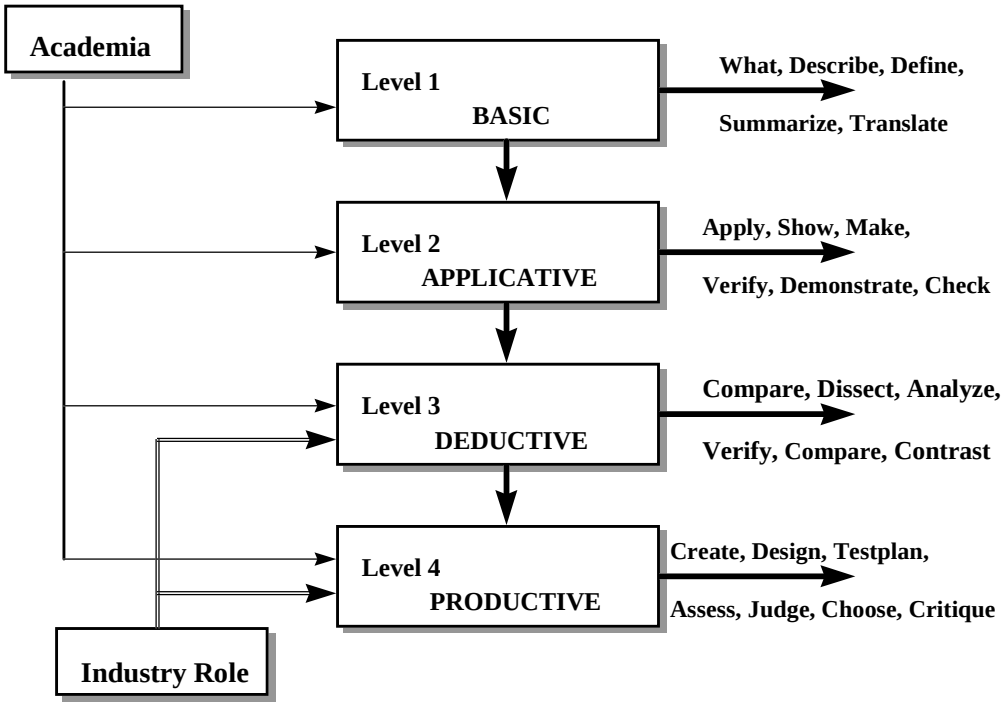


Figure 2. The Education Maturity Model (EMM)

The underlying ideas that motivate the EMM, illustrated in Figure 2, indicate that Level 1 (basic) can be supported by typical classroom instruction and presentation, Level 2 (applicative) can be supported by hands-on laboratories that make use of point tools (e.g., a VHDL simulator) to perform simple example problems, Level 3 (deductive) can be supported by advanced hands-on labs and notes describing the design of an advanced subsystem(s), and the most advanced level, Level 4 (productive), can be supported by material that allows the hands-on design and prototyping of actual complex systems through the use of tools and through evaluation of various tradeoffs. Level 4 educational material prepares the student, with little additional on-site training, for an immediate role as a productive engineer in industry or government. Often a particular industry may hire engineers educated to Level 3, and provide on-site courses to raise the level of knowledge to Level 4. Level 4 does not stand alone but requires "Level 3 understanding" in a number of related areas of specialization, as it deals with aspects of the complete system.

The Educational Maturity Model (EMM) allows organizations to develop and evaluate training material at each of the levels. Currently, very little is done in the typical university classroom beyond Levels 1 and 2. Levels 3 and 4 are primarily outcomes of knowledge gained in industry, and would greatly benefit the quality of education in the engineering area where it included in the university curricula. Cooperative industrial training, where the student spends summers in industry, is often an attempt to substitute for Levels 3 and 4.

In our efforts as part of the RASSP program, in addition to Levels 1 and 2, we have attempted to ensure that the material produced would support education at Levels 3 and 4. To accomplish this, the RASSP E&F team has developed a novel module-based framework. Similar to the knowledge unit concept proposed by the Joint Curriculum Task force [1], modules are developed on specific topics and then used in the development of a new course or for updating an existing course. The attractiveness of this approach is that it is easy to insert new material into an existing course or change the emphasis of a course through the use of modules. Likewise, it is easy to develop a new course that is customized towards a specific set of goals by grouping together a collection of modules. These capabilities are extremely useful in overcoming the traditional difficulty that instructors have in inserting new material into existing courses or curricula as described in Section 2.

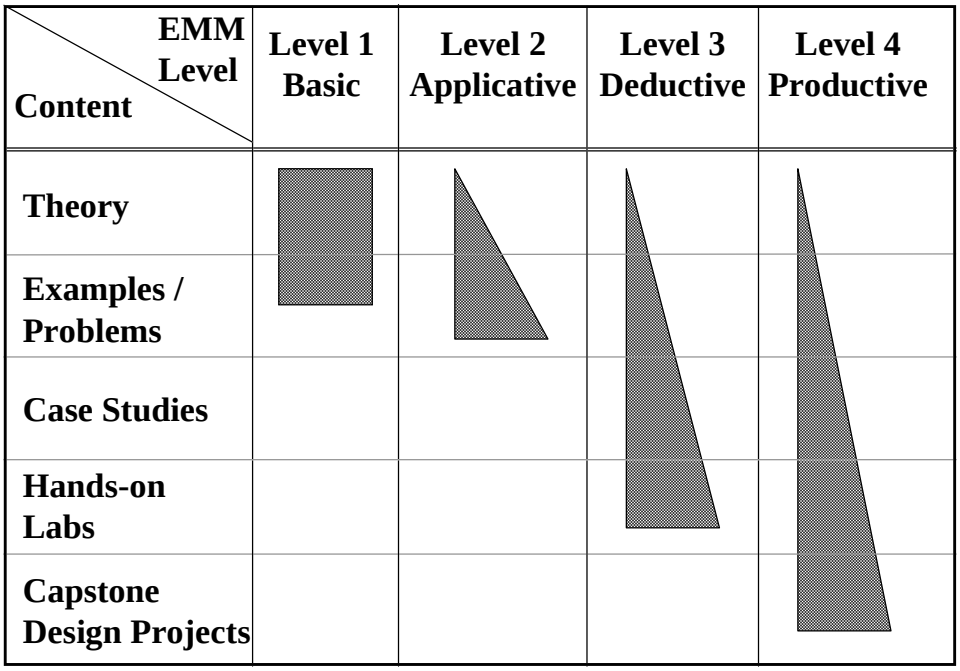


Figure 3. Relating EMM to the Content and Focus of Educational Material (Width of Triangles Indicate Relative Strengths of the Content and Level)

3.3 Module Overview

Each module consists of a comprehensive discussion of one technical sub area, (e. g., virtual prototyping) and presents the technical details, examples, and cases studies needed to obtain a thorough understanding of the topic. Each module represents a unit of a course that is independent of other modules in the course (aside from prerequisite requirements). A typical

module is designed to provide three hours of lecture time. As illustrated in Figure 3, a module provides Level 3 material through detailed hands-on labs, and notes that describe actual design projects (i.e., case studies). Level 4 is achieved through a capstone design project that is a comprehensive hands-on top-down design laboratory that covers the entire system design process and spans several modules.

There are many advantages to encapsulating a focused amount of material in a modular fashion. These include:

- Modules can be used in a "mix and match" scenario, depending upon the particular area of digital system design as well as the target audience needs;
- As technology advances in an area, only modifications to applicable modules are necessary. This approach reduces the cost of upkeep and makes it easier to keep pace with the rapid pace of technological change;
- Easy to develop a new course that is customized towards a specific set of goals by grouping together a collection of modules;
- Modules can be easily incorporated into existing graduate or advanced undergraduate courses within a university or into professional education courses in a university or industry;
- Modules are a mechanism for leveraging the efforts of other educators enabling reuse.

Several of these advantages are illustrated in Figure 4 below.

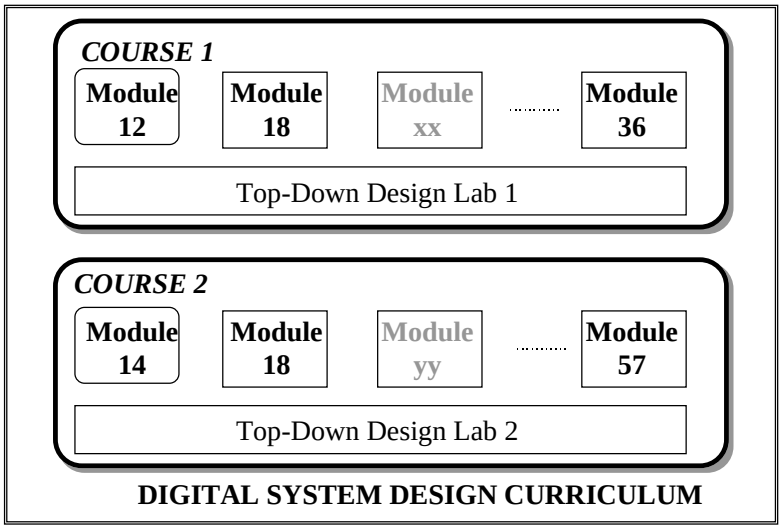


Figure 4. A comprehensive digital system design curriculum constructed as a series of courses, each of which contains modules at EMM Levels 1-4

A typical module, illustrated in Figure 5, consists of four components. The first component is the fundamental theory underlying the topic being covered. For example, in the module on Test Technology, the theory includes a discussion of the test problem, test generation and fault simulation theory, and design for testability techniques. The second component consists of examples and problems. This component provides simple examples that illustrate the theory and provides problems that can be used for homework exercises. The third component of a module is a hands-on laboratory exercise. The laboratory exercise is intended to rigorously demonstrate the

concepts taught in the other sections of the module by providing an opportunity to apply those theories on a significant problem in a learn by doing fashion.

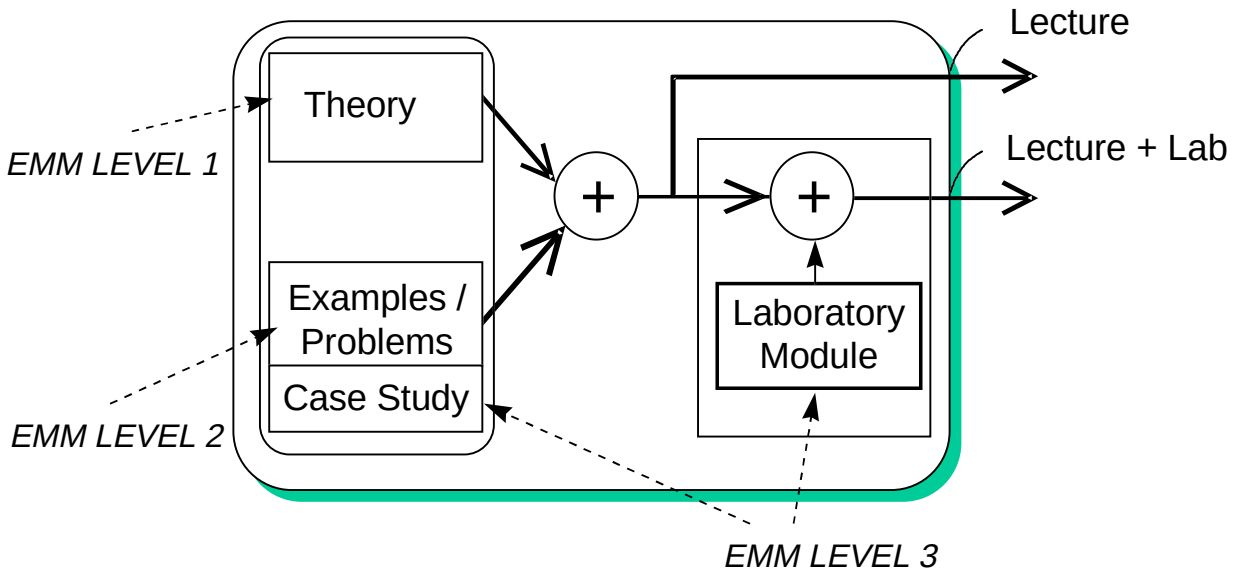


Figure 5. Module Organization

3.4 The RASSP Digital System Design Curriculum

Figures 6 illustrates our approach to the development of a comprehensive set of modules covering the RASSP design process. Each phase of the RASSP system design process is captured in one or more modules. A sequence of 8 – 10 modules augmented with a comprehensive system-design laboratory at EMM Level 4, form a quarter or semester university course. Figure 6 describes how a RASSP curriculum can be formed from a number of modules. The instructor is given the flexibility of tailoring the course to the desired goal, or introducing a few RASSP modules within his current course to augment it quickly and effectively.

One of the major challenges in the development of the RASSP modules was determining which modules should be developed. Initially, a large list of topics that comprised the core of new RASSP technology was prepared. These topics were then clustered into a few composite areas of knowledge which represented candidate topics for modules. Topics were selected based upon two criterion, which topics represented the key technical contributions of the RASSP activity and that background material which was necessary to understand the RASSP activity and not generally available in today's university curricula.

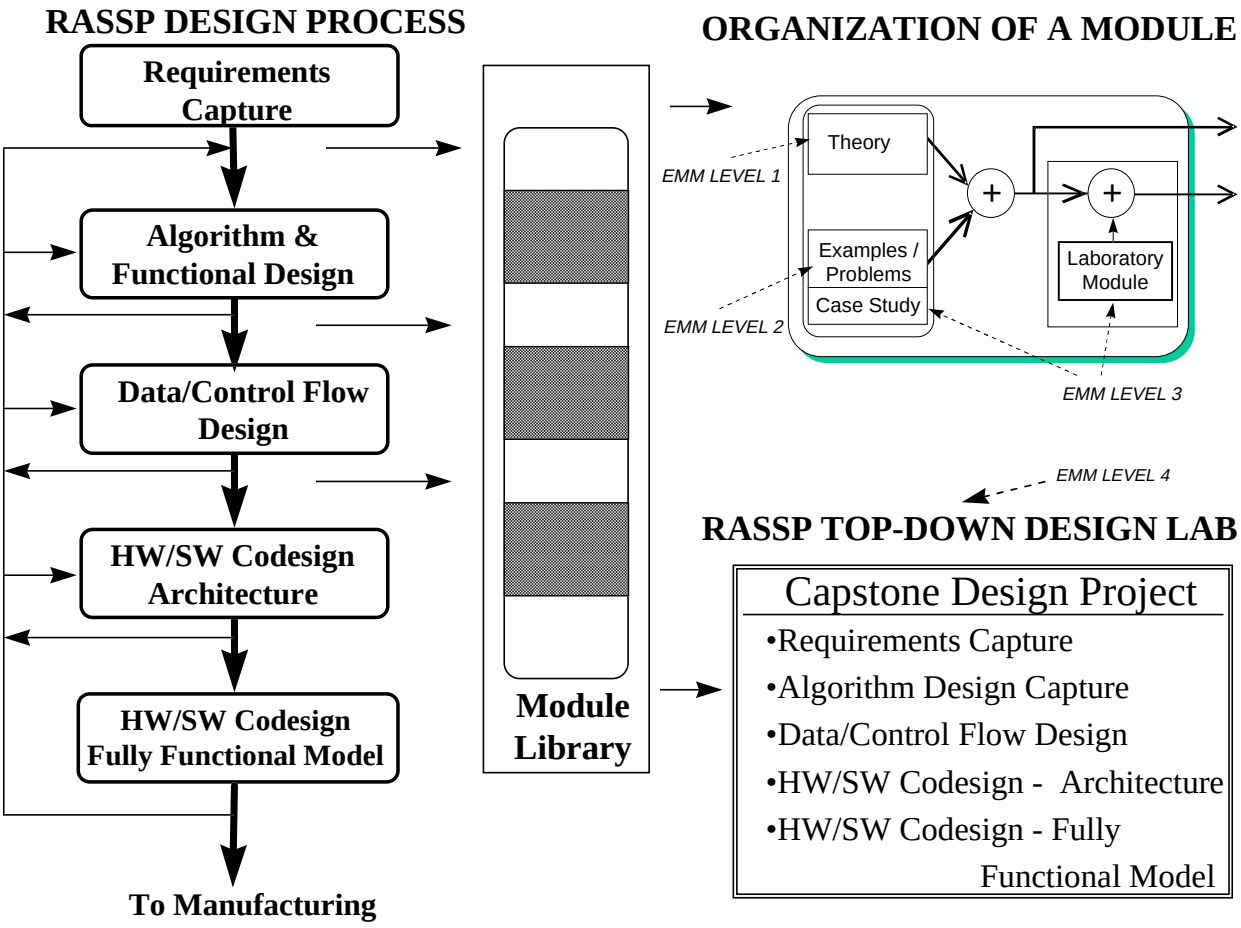


Figure 6: RASSP System Design Process is Captured in Modules, that Support EMM Levels 1-3, a RASSP Top-Down Laboratory Supports EMM Level 4

The following represents the list of modules developed by the RASSP E&F program (complete with Powerpoint slides, laboratories, problems and notes). These modules are available to instructors for use in their curricula via <http://rassp.scra.org/>. Note that new modules currently under development are shown in italics and are scheduled for completion in Summer 1997.

- **VHDL Basics:** an introduction to the VHSIC Hardware Description Language (VHDL), IEEE Std 1076-1993, and its fundamental concepts.
- **Structural VHDL:** a description of the use of VHDL in describing models in terms of component instantiations and interconnections.
- **Behavioral VHDL:** a description of VHDL features that can be used to describe the outputs of a component in response to changes in its inputs.
- **Advanced Constructs in VHDL:** a description of the constructs in VHDL that are more reminiscent of high-level programming languages such as file I/O, abstract data types, shared variables, etc.
- **System Level Modeling:** an introduction to techniques used for modeling systems at a high level (CPU, Memories, Interconnect, etc.) in a top-down design process.

- **Hardware/Software Codesign:** an introduction to the concepts of codesign (concurrent design) of hardware and software, from specifications, for embedded systems.
- **Hardware/Software Partitioning:** an introduction to the techniques used, in the design of embedded systems, to determine which functions are to be implemented in software on COTS processors and which are to be implemented in hardware (ASICs) and the trade-offs associated with such a partitioning.
- **DSP Architectures:** a description of various computation, communication, I/O, software, test, and maintenance architectures for embedded digital signal processors.
- **Scheduling & Assignment for DSP:** methods for allocation, scheduling and assignment of a set of software tasks in a DSP application to a selected hardware architecture.
- **DSP Algorithm Design:** a description, including examples, of a number of simulation-based functional and timing design and verification environments for design of digital signal processing algorithms.
- **Communication Protocols:** a presentation of selected communications protocols for DSP architectures geared towards understanding the relationship between them and overall system performance.
- **RASSP Methodology Overview:** an introduction to the RASSP program including a comparison of pre-RASSP and current RASSP design methodologies.
- **Virtual Prototyping for DSP Architectures:** a description of virtual prototyping (simulation based design) as applied to the design of DSP systems. Included are executable specifications, algorithm development, architecture selection, detailed design and implementation and test.
- **Virtual Prototyping using VHDL:** A discussion on how a virtual prototyping based top-down design flow is realized in VHDL. A complex design example is presented showing detailed integration and test.
- **Hardware Synthesis Overview:** an introduction on the concepts of hardware synthesis including definitions, how synthesis tools function, and general coding styles for successful hardware synthesis.
- **Libraries: Generation, Maintenance, Reuse Overview:** an overview of problems that inhibit hardware/software reuse practice and current solutions for them. A survey of reuse metrics and a tool that tracks them is also presented.
- **Test Technology Overview:** a presentation of the fundamentals of digital systems testing including fault modeling, test generation and fault simulation algorithms, and design for testability and built-in self test techniques.
- *Requirements and Specifications Modeling:* a description of how executable specifications are derived from customer requirements, and a description of how they drive the top-down design process through regression testing.
- *Performance Modeling using VHDL:* a presentation of the environments that exist for doing simulation based performance modeling using VHDL. A discussion of hybrid modeling – the simulation of mixed performance and behavioral models – is included.
- *Enterprise Integration:* a presentation on the supporting EDA infrastructure, tool/configuration management rationale, workflow methodologies, and distributed collaboration and design environments, utilized in a top-down system-level design process.

- *Cost Analysis for Design:* a discussion of how quantitative and empirical cost models for design, implementation, test maintenance, and production can be utilized in the front-end design of embedded digital systems, in a concurrent engineering approach.
- *Robust Design for Quality:* a presentation on how products can be designed for 6-sigma quality. Included are state-of-art discussions on Taguchi methods, Monte Carlo methods, surface response, and fuzzy set methods for improving quality of products by improving their tolerance to process parameter variations with case studies.
- *Project Management:* this presentation covers the scheduling, administrative, workflow, financial, and customer-support related issues in managing large electronics system design projects.
- *Design for Manufacturing:* a description of how products and processes are designed for ease of manufacture.
- *Implementation Technologies:* a description of the various technologies available for implementation of digital systems including trade-offs and changes in the design process for them. Included are FPGAs, ASICs, Custom ICs, and MCMs**.**

These modules have been used in the creation and delivery of courses at the University of Virginia, the Georgia Institute of Technology and the University of Cincinnati. Today, more than 80 academic institutions have obtained modules for use within their new and existing courses.

To support the use of these modules, the RASSP E&F group has organized several "teach the teachers" workshops that were designed to educate university faculty on the content of the modules covered and how they may effectively and efficiently utilize this information.

Currently, the RASSP E&F group has scheduled an Educators Workshop which will present a group of modules and provide the material to the attendees. The modules that are will be presented include; Executable Specifications, Cost Modeling in Design, Performance Modeling using VHDL, Hardware/Software Codesign, Hardware/ Software Partitioning, and Virtual Prototyping using VHDL. Additional modules such as the VHDL modules, Hardware Synthesis, and Test Technology Overview will be briefly summarized and made available to the attendees. This workshop is scheduled for August llth-14th, 1997. The RASSP E&F group is also helping to organize the first IEEE Computer Society International Conference on Microelectronics Systems Education. This conference is being organized using the model of the VLSI Educators Workshops held by NSF in the '80s. Its purpose is to provide a forum for educators to share experiences and techniques for introducing the principals of modern digital system design concepts into the academic curriculum. This conference is scheduled for July of 1997, in Washington D.C. < http://www.cedcc.psu.edu/mse97/>.

An example of the flexibility of the module concept is illustrated by the use of the modules developed by the RASSP E&F team to develop an IEEE VHDL Interactive Tutorial CD-ROM. This tool was developed based upon several of the VHDL modules developed by the RASSP E&F team. The objective was to provide a complete, user-friendly reference to the VHDL language which is an important part of the RASSP process. This CD contains a hyper-linked

version of the VHDL LRM integrated with hyper-linked versions of the VHDL modules described above. For more information see <http://rassp.scra.org>.

4. National Digital Design Archive

The Educational Maturity Model (EMM) as discussed in the earlier sections of this paper, allows a synergistic effort in both the creation, testing, and archiving of the educational material relating to new technology developments. We have also recently proposed the creation of a national digital design archive that would utilize the best of technology and the WWW in addressing issues of quality, review, and comprehensiveness of the library-based environment. These are some of the benefits that would be derived from the establishment and acceptance of a National Digital Design Archive:

1. Rapid growth of new technologies and their short lifetimes requires a coordinated effort between universities and the industry to develop a curriculum that is relevant to the national needs. No classification of the levels of educational material appears to be in use, leading to the unavailability of educational material in technological fields commensurate with unique needs.
2. No readily available "clearing house" for educational information such as course modules, design laboratories and system models, tools, and case studies, exists. While several efforts, sponsored by NSF and other organizations, aimed at virtual WWW libraries exist, very little is present at classifying the types of educational material available or determining their relevance.
3. Very little credit is available to faculty members or to the industry for creating new educational material or in creating detailed case histories of past projects. In addition, if an engineer in the industry creates an educational module, she is not sure how it could be introduced to the general academic community, or how it can be reviewed for completeness.
4. Free flow of technical information between academia and industry is not organized nor does it follow a timely and standardized format. Conferences, licensing, patents, and other passive approaches require long timelines and may not achieve the necessary results.

To ensure the formatting consistency and material correctness and relevance, the course modules, simulation tools, and interactive laboratories, will now undergo a systematic classification and review process before being incorporated into the design archive. As more details are available, they will be post at http://rassp.scra.org.

5. Summary

In this paper we have outlined an effective process to ensure that technology education in Electrical Engineering remains relevant to the needs of the society. A cooperative approach between industry, academia, and government, in solving some of the problems with respect to effective technology identification, creation, and its proliferation was discussed together with a new Educational Maturity Model (EMM) to assist educators and the user community in benchmarking the educational material available. A comprehensive digital system design education curriculum developed as part of DARPA's RASSP program is also introduced.

Finally, a proposal for a national archive for digital design education is proposed, and preliminary steps outlined.

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Biography

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