

”Design of Integrated 5G Chip-set with Microstrips Modules for Mobile Communications with Its Integration in MMIC Course”

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Design of Integrated 5G Chip-set with Microstrips Modules for Mobile Communications with its Integration in MMIC Course

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Abstract -With the surge in global usage of internet in smartphones, so has the need for extra Bandwidth requirements with simultaneous shared antenna capabilities for multi-channel video streaming and data speeds up surged. In order to meet design specifications two different ECADs namely ADS and AWR were used based on the High Frequency Engineering Design requirement and to obtain accurate RF results. A comprehensive design of RF Wilkinson Power Divider (WPD) incorporating microstrip lines in two-sectional configuration including EM model testing for device modeling, using RF test bench consisting of Fitted and Discrete frequency interpolation points have been carried out. Receiver (RX) System modeling results using 1-tone and 2-tone RF signals are meticulously presented along with analytical results for RX System analysis and synthesis. Exhaustive simulations have been carried out in all cases along with comparisons using ADS as the primary software tool. During these investigations the theoretical and simulation results are found to be in good agreement at System level, including design validation and modeling of the integrated RX module.

The design of Bandpass Filters (BPF), Quadrature (90°) Hybrid Branch Line Coupler (BLC) incorporating microstrips and a 3 dB filter in four port network configuration has been carried out. It incorporates the EM model for device modeling, using Full-wave analysis consisting of Fitted and Discrete frequency interpolation points. Comprehensive RF Power Analysis and Optimizations of Radio Link with the modeling results achieved by Small and Large Signal analysis are meticulously presented. During the investigations carried out using the ADS Harmonic Balance tool for Noise control, the hypothetical simulation results are found to be in good agreement at System level. These include design validation and modeling effects of the integrated RX System Front End module for 5G Communications. An introduction to establish a common level of knowledge at System level platform is also addressed. Frequency response definitions of conventional BPF for 3rd order Chebyshev type – I filter approximations are discussed. In the end, the derivation of S-parameters matrix for the BLC carried out using the well-known Even-Odd mode network analysis is presented.

1. INTRODUCTION

During the 5G investigations, eight modules have been built mostly based on the Fundamentals of Physics, Semiconductors and Circuit Theory including the Patch Antennas, BPF, Couplers, Transmitter (TX), Receiver (RX) and Switches etc. The Switch between the Antenna and TX and/or RX must be equipped to handle high power when connected to the TX, and LO-Power when connected to the RX. In order to meet these requirements, the p-i-n diodes with forward and reverse biases have been used, respectively. Its Phase

shifting capability is deployed while designing the Antenna. The Varactor diode is used in designing wideband BPF because the diode resonates at frequencies at the application of different reverse biased modes. All principles of Device Physics, Semiconductor Fundamentals and Circuit Theory are integrated in the Author's MMIC Design and Fabrication Course.

During these research investigation eight modules have been built mostly based on the Fundamentals of Physics, Semiconductor, and Circuit theory. Only few modules, however, are covered here in details deployed at the receiver as well as the transmitter end. Front end receiver (RX) employs patch antenna, SPDT switch, low noise amplifier (LNA), mixer with oscillator, band pass filter (BPF), power limiter and (ADC) modulator.

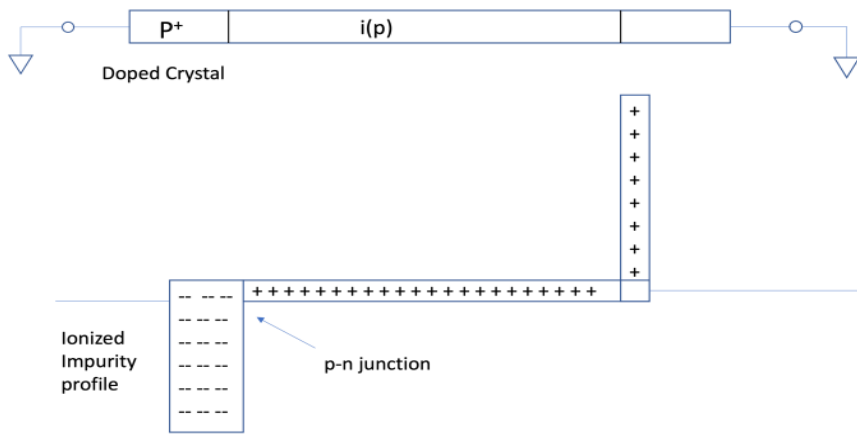
The transmitter (TX) uses (DAC) demodulator, mixer with oscillator, power amplifier (PA), BPF and SPDT switch attached to the patch antenna. In order to transmit the maximum power matching networks are used. All the elemental values R, L and C are built with microstrips such as microstrips lines (MLIN), microstrip coupled lines (MCLIN) and microstrips thin film capacitors (MTFC), and microstrip coupled line filter (MCFIL), microstrip inductor (MSIND) etc. as given in ADS [1]

A novel SPDT switch is designed which is capable of handling very high power from the TX and very low power to the RX. The P-i-N diode is chosen for this purpose, which handles very high power in its forward biased state, and a very low power at its reverse biased state.

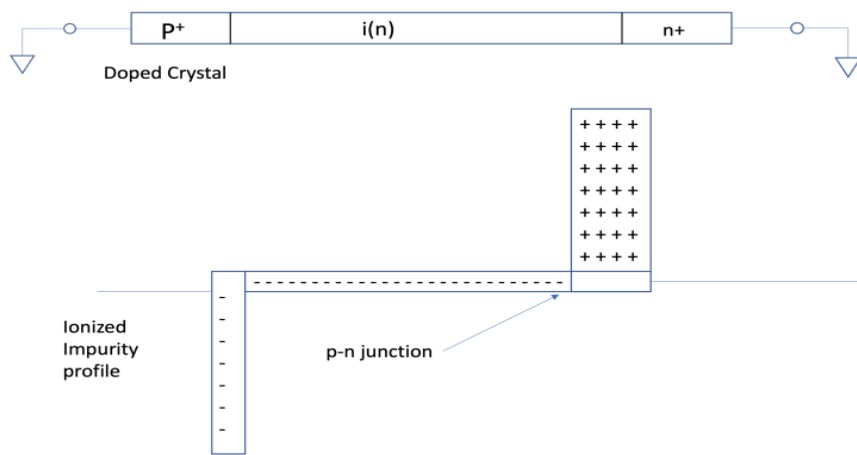
A radio system is comprised of discrete modules essential for the receiver (RX) and the transmitter (TX) architecture. The Heterodyne principle is accomplished by integrating the discrete RF modules and performing modeling at system level using RF base band intermediate frequency (IF), and carrier frequency (RF) as a single sideband (RF-IF) = LO frequency. Conventional wireless communicator systems were established on high power TX units with the RF unit functional up until the signal levels decreases below a certain noise level (Threshold). However, with adjacent systems operating at same frequencies were found to be sensitive to interferences. Thus, system transmitting at identical frequencies were physically separated so that signals fall below the established noise threshold before interference occurs [2]. The physics and mathematics along with their models of all eight 5G modules are thoroughly covered in the MMIC Design and Fabrication course by the author. However, only selected few modules of high importance with examples are depicted in the paper with the ADS based design and simulation results.

2. P-i-N DIODE with APPLICATIONS

Figure 1 depicts the p-i-n diode along with its profiles. Since the width of the depletion region is inversely proportional to the resistivity (doping concentration). The wider depletion region amounts to a smaller junction capacitance. The i- region consists of impurities either p-type or n-type. The i region is of sufficiently high resistivity so that few impurities in the region are ionized and the depletion region extends throughout the i- region and includes a small penetration into both the $p+$ and $n+$ regions as shown in Figure 1 (ii). Because of the heavy doping of the $p+$ and $n+$ regions, the depletion does not extend very far into them, and the depletion width is essentially equal to the i- region width. The junction capacitance in the reverse bias is determined by this width [3].



(i)



(ii)

Figure 1 Profiles of two types of P-i-N Diodes

Packed P-i-N diode

The equivalent circuit of P-i-N region can be represented as shown in FIGURE 2.

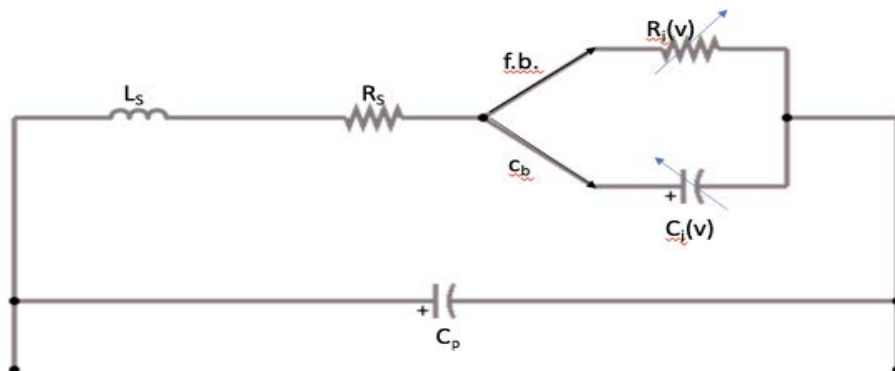
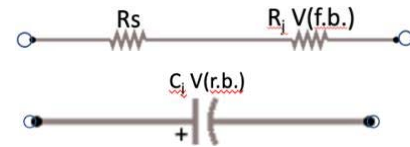


Figure 2 Equivalent Circuit of a P-i-N Diode

The arrows connected to variable R_g are in forward bias and C_g in reverse bias. R_s is a very small resistance connected to the diode. $R_g(V)$ is the variable resistance of the diode, which has very small value with the forward bias, but a very large resistance with reverse bias. (V) is the double capacitance whose value is dependent at the reverse bias. The L_s and C_p are inductance and capacitance of the package. Neglecting the package effects of L_s and C_p , the equivalent circuit with forward bias behaves like a short circuit with total resistance $R_T = R_s + R_j$ (f.b.)

Whereas the circuit with reverse bias acts as an open circuit.



Since Z_c in reverse bias is much higher than the 50Ω transmission line impedance.

Calculations for Isolation and Insertion losses:

These calculations [5-9] are based on extracting A, B, C and D circuit parameters and applying them to the S parameters at microwave. The basic building blocks for series impedance 'Z', the parallel admittance 'Y', and lossless transmission line with a characteristic impedance Z_0 and length l are given by as follows:

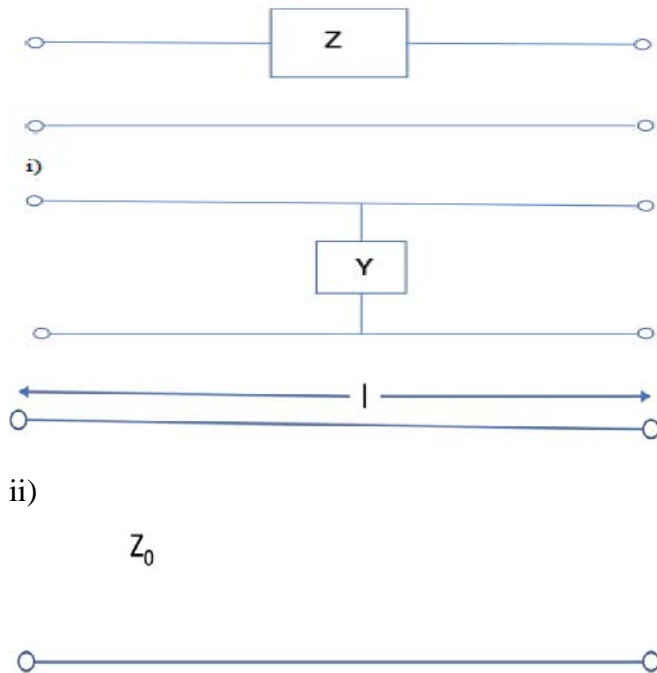


Figure 3 Three Basic Building Blocks

The ABCD matrix for $Z=R + jX$ is given in Figure 3 (i)

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix}; \text{ Where } A = 1, B = Z, C = 0, D = 1$$

The ABCD matrix for $Y=G_T + jB$ is given in figure 3 (ii)

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix}; \text{ Where } A = 1, B = 0, C = Y, D = 1$$

The ABCD matrix for lossless transmission line is given in Figure 3 (iii)

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\beta l & jZ_o \sin\beta l \\ jY_o \sin\beta l & \cos\beta l \end{bmatrix}$$

Where $A = \cos\beta l$; $B = jZ_o \sin\beta l$
 $C = jY_o \sin\beta l$; $D = \cos\beta l$

By definition S_{21} is the transmission coefficient of S-matrix, which is given

$$S_{21} = \frac{2}{A + BY_o + CZ_o + D}$$
 from transmission table of S vs ABCD parameters

So for $Z = R + jX$ $S_{21} = \frac{2}{1 + \frac{(R+jx)}{Z_o} + 1} = \frac{1}{1 + \frac{R}{2Z_o} + \frac{jx}{2Z_o}}$

So Attenuation ' α_L ' = $\left| \frac{1}{S_{21}} \right| = \left| 1 + \frac{R}{2Z_o} + \frac{jx}{2Z_o} \right|$
 $\left[\left(1 + \frac{R}{2Z_o} \right)^2 + \left(\frac{x}{2Z_o} \right)^2 \right]^{\frac{1}{2}}$
 $1 + \frac{R}{2Z_o}$ which with forward bias as $x = 0$, so Attenuation = $1 + \frac{R_s + R_g}{2Z_o}$

Where α_L is defined as $20 \log \left| \frac{1}{S_{21}} \right|$, so

$$\alpha_L = 20 \log \left[\left(1 + \frac{R_s + R_g}{2Z_o} \right)^2 \right]^{\frac{1}{2}} = 20 \log \left(1 + \frac{R_s + R_g}{2Z_o} \right)$$

In case of reverse bias $R = R_r$, and $X = \frac{-j}{\omega C}$ so α becomes

$$\alpha = \left| \frac{1}{S_{21}} \right| = \left(1 + \frac{R_r}{2Z_o} \right)^2 - \left(\frac{j}{4\pi f C_g Z_o} \right)^2$$
 which is isolation

$$\alpha_i = 10 \log \left[\left(1 + \frac{R_r}{2Z_o} \right)^2 + \left(\frac{1}{4\pi f C_g Z_o} \right)^2 \right]$$

Essentially, P-i-N diode provides minimum insertion loss with forward bias maximum isolation with reverse bias. This provides sound platform in switching applications with adequate power handling capabilities. Input power is usually expressed in dBm i.e., P_{dBm} , so output power P_0 can be expressed as $P_0 = P_i - \alpha L$ in ON state of the p-i-n diode. For OFF state, the p-i-n diode is reverse biased. The isolation is expressed in dBs. So, output power is expressed as $P_0 = P_i - \alpha_i$.

2.1 Circuit Modules of a Packaged P-i-N Diode

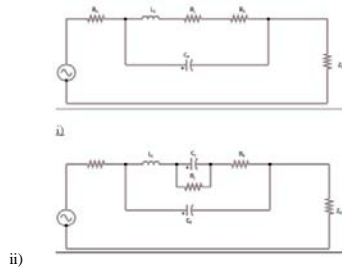


Figure 4. Equivalent Circuits at i) Forward Bias ii) Reverse Bias

At forward bias, the diode acts as nearly short circuit which causes the microwave power to be reflected totally. As shown in Figure-4 (i) the switch is ON and the insertion loss is:

$$\alpha = \alpha L = 10 \log \left[\left(1 + \frac{R}{2Z_o} \right)^2 + \left(\frac{X}{2Z_o} \right)^2 \right];$$

$$\text{Where } Y_D = j\omega C_P + \frac{1}{R_S + j\omega L_S}$$

$$Z_D = \frac{1}{Y_D} = R + jX$$

At reverse bias, the diode acts as a nearly open circuit, the signal passes through the microchip line with an insertion loss αL which is due to the finite value of C_p . As shown in Figure-4 (ii) the switch is OFF and the isolation is

$$\text{Now } R_S + j\omega L_S + \frac{1}{\left(\frac{1}{R_g}\right) + j\omega C_g}$$

$$Y_D = j\omega C_P + \frac{1}{R_S + j\omega L_S + \frac{1}{\left(\frac{1}{R_g}\right) + j\omega C_g}}$$

$$\text{So } Z_D = 1/Y_D$$

$$\text{So } \alpha = \alpha_i = 10 \log \left[\left(1 + \frac{R}{2Z_o}\right)^2 + \left(\frac{X}{2Z_o}\right)^2 \right]$$

All these concepts pertaining to p-i-n diode have been successfully integrated into course EECE 517 MMIC Design and Fabrication. The detailed calculations for insertion loss and isolation along with simulation are carried out making use of ADS tools in the classroom along with intensive analytical techniques. Some select examples are being presented in this paper spectral analysis phase shift αL and α_i in dBs along calculating minimum detectable signal levels at input and output.

Example #1 [6]

A nonlinear mixer diode is used as an up converter shown in Figure 5. Assume that the output current of the diode is $i = a_0 + a_1V + a_2V^2$. Where $v = v_{RF} \sin(\omega_{RF} t) + v_{LO} \sin(\omega_{LO} t)$; $\omega = 2\pi f$. Calculate the frequencies of all signals at port A in the diagram. Draw a composite spectrum for all the frequencies along with their amplitudes.

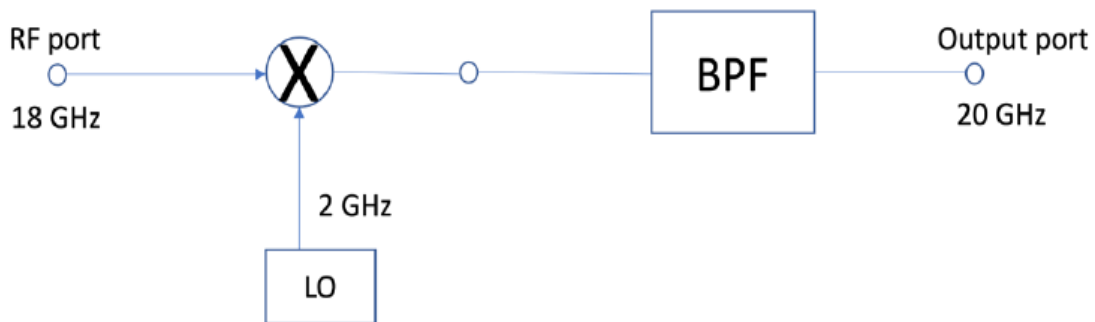


Figure 5. Up Converter Mixer with LO.

Apply $v = v_{RF} \sin(\omega_{RF} t) + v_{LO} \sin(\omega_{LO} t)$ into (i)

$$i = a_0 + a_1 (v_{RF} \sin(\omega_{RF} t) + v_{LO} \sin(\omega_{LO} t)) + a_2 [v_{RF}^2 \sin^2(\omega_{RF} t) + 2 v_{RF} v_{LO} \sin(\omega_{RF} t) \sin(\omega_{LO} t) + v_{LO}^2 \sin^2(\omega_{LO} t)] \quad \text{-----(1)}$$

Making use of identities $\sin^2 \theta = (1 - \cos 2\theta) / 2$ and

$\sin \theta_1 \sin \theta_2 = [\cos(\theta_1 - \theta_2) - \cos(\theta_1 + \theta_2)] / 2$ and substituting for i,

$$i = a_0 + a_1 v_{RF} \sin(\omega_{RF} t) + a_1 v_{LO} \sin(\omega_{LO} t) + \frac{1}{2} a_2 v_{RF}^2 (1 - \cos(2\omega_{RF} t)) + a_2 \frac{2}{2} v_{RF} v_{LO} (\cos(\omega_{RF} - \omega_{LO}) t) \quad \text{-----(2)}$$

$- \cos((\omega_{RF} + \omega_{LO}) t) + \frac{1}{2} a_2 v_{LO}^2 (1 - \cos(2\omega_{LO} t))$ collecting coefficients.

$$i = a_0 + \frac{1}{2} a_2 v_{RF}^2 + \frac{1}{2} a_2 v_{LO}^2 + a_1 (v_{RF} \sin(\omega_{RF} t) + v_{LO} \sin(\omega_{LO} t)) + a_2 v_{RF} v_{LO} \cos((\omega_{RF} - \omega_{LO}) t) \quad \text{-----(3)}$$

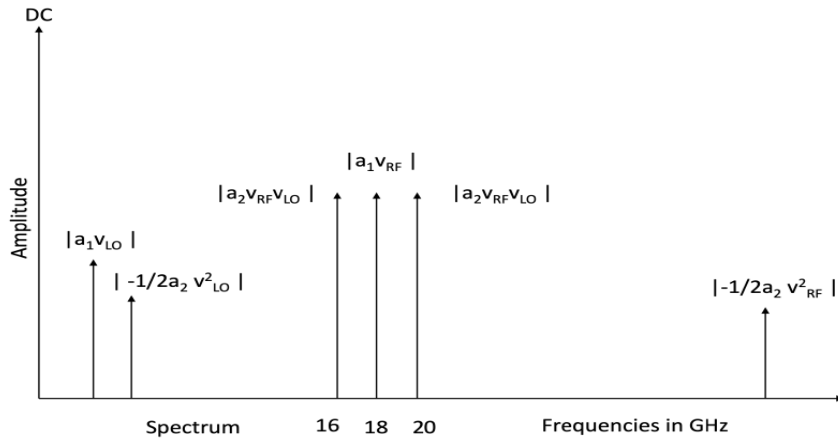
$- a_2 v_{RF} \cos((\omega_{RF} + \omega_{LO}) t)$

From (3) the spectrum is obtained at frequencies

DC	f_{RF}	f_{LO}	$2f_{RF}$	$2f_{LO}$	$f_{RF} = f_{LO}$	$f_{RF} \pm f_{LO}$
0	18	2	36	4	10	20

The results of equation (3) along with fundamental, harmonics and amplitudes are given in tabular form as below:

S. No.	Component	Frequency	Amplitude
1.	D.C.	0 Hz	$a_0 + 1/2 a_2 (v_{RF}^2 + v_{LO}^2)$
2.	f_{LO}	2 GHz	$a_1 v_{LO}$
3.	f_{RF}	18 GHz	$a_1 v_{RF}$
4.	$2f_{LO}$	4 GHz	$-1/2 a_2 v_{LO}^2$
5.	$2f_{RF}$	36 GHz	$-1/2 a_2 v_{RF}^2$
6.	$f_{RF} = f_{LO}$	16 GHz	$a_2 v_{RF} v_{LO}$
7.	$f_{RF} \pm f_{LO}$	20 GHz	$a_2 v_{RF} v_{LO}$



Example #2 [6]

Derive the phase shift Φ and the attenuation α for the circuit shown in Figure F.

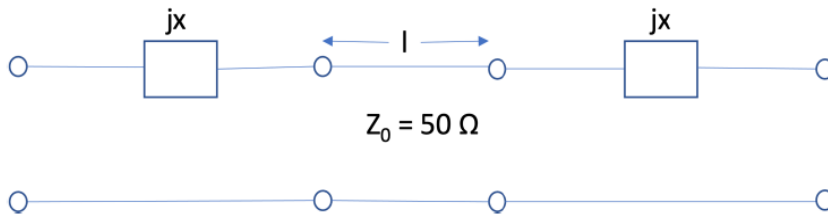


Figure 6 Phase Shifter and Attenuator

Transmission line is lossless with $Z_0 = 50\Omega$ and electrical length $= \beta l = \theta$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & jX \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \cos\theta & jZ_0 \sin\theta \\ jY_0 \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} 1 & jX \\ 0 & 1 \end{bmatrix}$$

$$= \begin{bmatrix} \cos\theta - XY_0 \sin\theta & j[2X \cos\theta + (Z_0 - X^2 Y_0) \sin\theta] \\ jY_0 \sin\theta & \cos\theta - XY_0 \sin\theta \end{bmatrix}$$

$$\text{So, } A = \cos\theta - XY_0 \sin\theta \quad B = j[2X \cos\theta + (Z_0 - X^2 Y_0) \sin\theta]$$

$$C = jY_0 \sin\theta \quad D = \cos\theta - XY_0 \sin\theta$$

$$\text{So, } S_{21} = \frac{2}{A + BY_0 + CZ_0 + D}$$

$$= \frac{2}{2(\cos\theta - XY_0 \sin\theta) + jY_0[2X \cos\theta + Z_0 + X^2 Y_0 \sin\theta] + j \sin\theta}$$

$$= \frac{1}{S_{21}} = \cos\theta - XY_0 \sin\theta + j\{Y_0[2X \cos\theta + (Z_0 - X^2 Y_0) \sin\theta + \sin\theta]\}$$

$$\text{So } \alpha = \left| \frac{1}{S_{21}} \right| = (\cos\theta - XY_0 \sin\theta)^2 + \frac{\{Y_0[2X \cos\theta + (Z_0 - X^2 Y_0) \sin\theta + \sin\theta]\}^2}{4}$$

$$A \text{ in dB} = 10 \log \left[(\cos\theta - XY_0 \sin\theta)^2 + \frac{\{Y_0[2X \cos\theta + (Z_0 - X^2 Y_0) \sin\theta + \sin\theta]\}^2}{4} \right]$$

$$\text{Here } \sum \text{Re} = \cos\theta - XY_0 \sin\theta$$

$$\sum \text{Im} = XY_0 \cos\theta + \left(1 - \frac{X^2 Y_0^2}{2}\right) \sin\theta$$

$$\varphi = \tan^{-1} \frac{\left(\frac{X}{Z_0}\right) \cos\theta + \left(1 - \frac{X^2}{2Z_0^2}\right) \tan\theta}{1 - \frac{X}{Z_0} \tan\theta}$$

This provides the basis of phase shifting.

Example #3 [6]

The receiver system shown in figure 7 below is operating with a RF input signal of 10 to 11 GHz. Calculate

a) The overall gain and loss of the system.

b) The overall noise figure in dB, and

c) The input and output minimum detectable signal levels in mW for the receiver at room temperature.

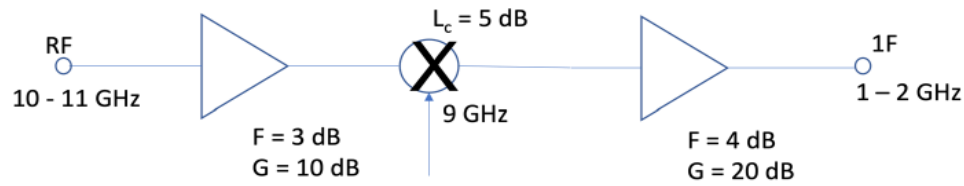


Figure 7 Receiver System

a) $G_T \text{ dB} = G_1 + G_2 + G_3 = 10 \text{ dB} + (-5 \text{ dB}) + 20 \text{ dB} = 25 \text{ dB}$

$L_T \text{ dB} = -25 \text{ dB}$

b) For noise figure F in dB

$G_1 = 10 \text{ dB} = 10, F_1 = 3 \text{ dB} = 1.9953$

$L_c = 5 \text{ dB}, \text{ so } G_c = -5 \text{ dB} = 10^{\frac{-5}{10}} = 0.3162$

$G_3 = 20 \text{ dB} = 10^2 = 100; F_3 = 7 \text{ dB} = 10^{\frac{7}{10}} = 2.519$

Noise Factor F_N

$$F_N = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2}$$

$$= 1.9953 + \frac{2.1623}{10} + \frac{1.5199}{10 \times 0.3162} = 2.6896$$

c) $P_{iMDS} = -111 + 10 \log \text{ BW} + F$

$$= -111 + 10 \log \frac{10 \times 10^9}{106} + 4.2969$$

$$= -76.7031$$

$$P_{iMDS \text{ mW}} = 10^{\frac{-76.7031}{10}} = 2.1364 \times 10^{-8} \text{ mW}$$

$$P_{iMDS \text{ mW}} = -76.7031 + 25 = -51.7031 \text{ dBm}$$

$$P_{iMDS \text{ mW}} = 10^{\frac{-51.7031}{10}}$$

$$= 6.756 \times 10^6 \text{ nW}$$

3. Wilkinson's Power Divider and Power Combiner

Wilkinson Power Combiner (WPC) is a 3-port network device often made using Microstrip lines. For 3-dB device operation, port isolation is achieved using quarter-wave transmission lines acting as microstrip arms followed by balancing these arms (output ports) using a balanced resistance with respect to the input port.

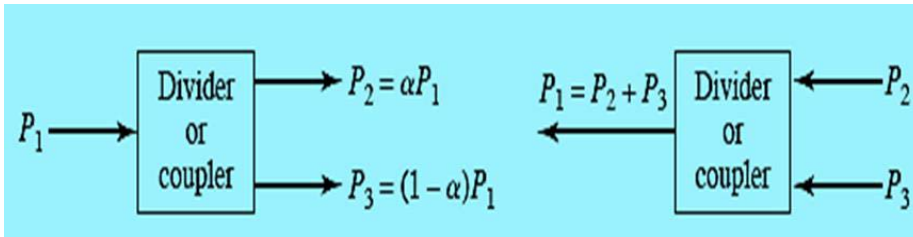


Figure 8. Power Coupler with Power Divider and Power Combiner

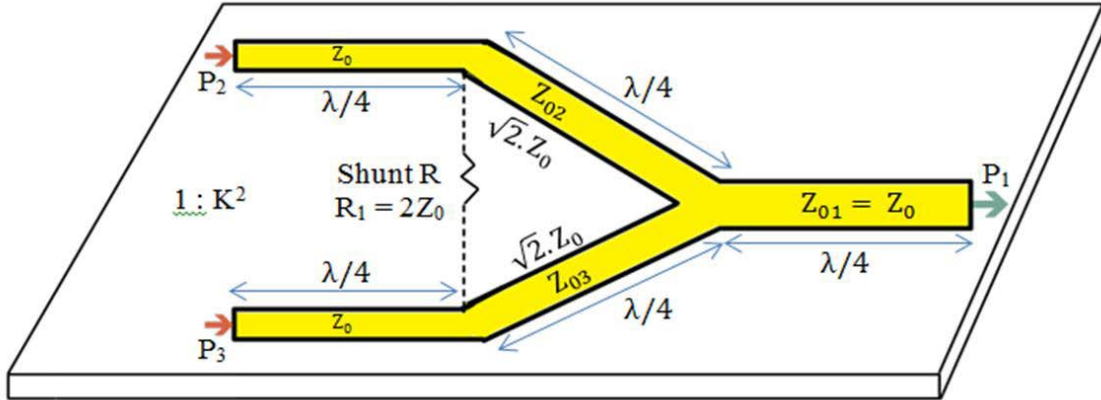


Figure 9. Geometry of Wilkinson's Power Combiner

Fig. 9 shows WPC structure whose analysis is made with Even-Odd mode coupling techniques that uses superposition theorem and network symmetry to deduce the ideal (lossless transmission line) [S] parameter matrix, given in [10,11] as

$$[S] = \frac{-j}{\sqrt{2}} \cdot \begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} = \begin{bmatrix} 0 & \frac{-j}{\sqrt{2}} & \frac{-j}{\sqrt{2}} \\ \frac{-j}{\sqrt{2}} & 0 & 0 \\ \frac{-j}{\sqrt{2}} & 0 & 0 \end{bmatrix}$$

A 3-dB Wilkinson Power Divider with a power division ratio of $1:K^2$ where $K = \sqrt{\frac{P_2}{P_3}} = 1$, i.e.

an equal power split (1:1 power ratio) and a source impedance of $Z_0 = 50 \Omega$ has the following

design expressions of impedances shown in Figure 9 taken from [5].

$$\text{Shunt resistor } R = Z_0 \cdot \left(K + \frac{1}{K} \right) = 2Z_0$$

$$Z_{03} = Z_0 \cdot \sqrt{\frac{1+K^2}{K^2}} = \sqrt{2} \cdot Z_0$$

$$Z_{02} = K^2 \cdot Z_{03} = Z_0 \cdot \sqrt{K \cdot (1 + K^2)} = \sqrt{2} \cdot Z_0$$

3.1 Distributed Model of WPD with Results

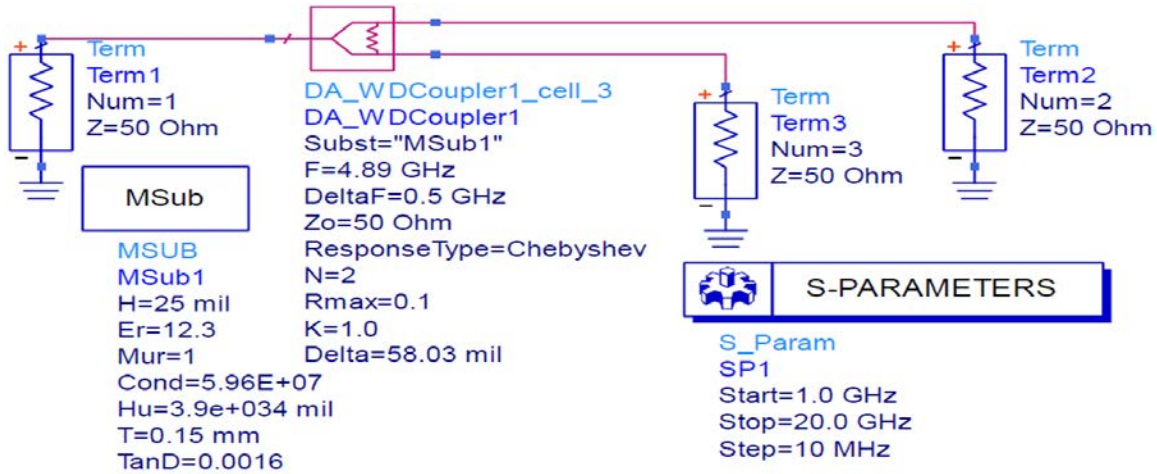


Figure 10. ADS Model with Microstrips

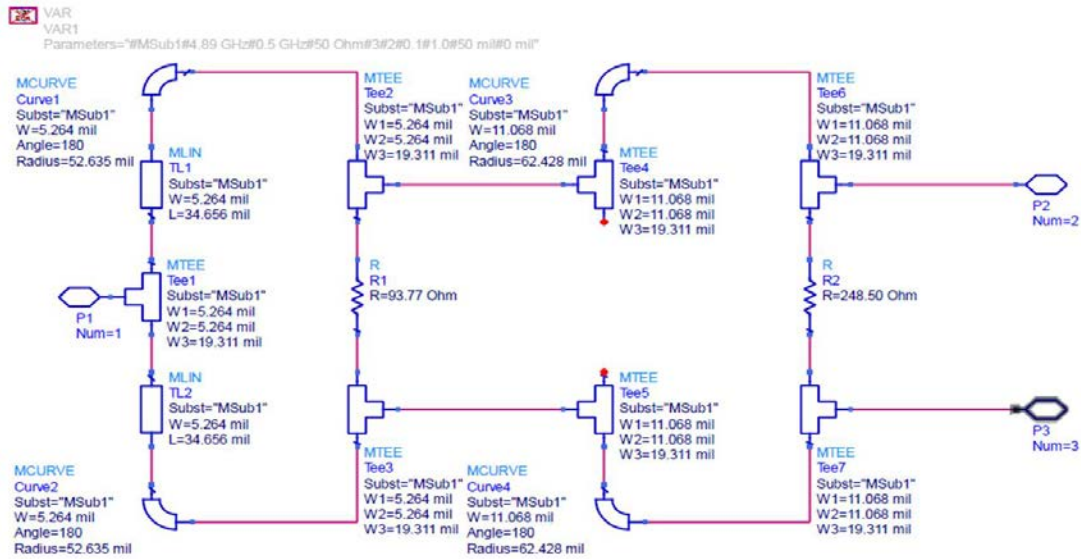


Figure 11. Schematic of Optimized WPD in ADS

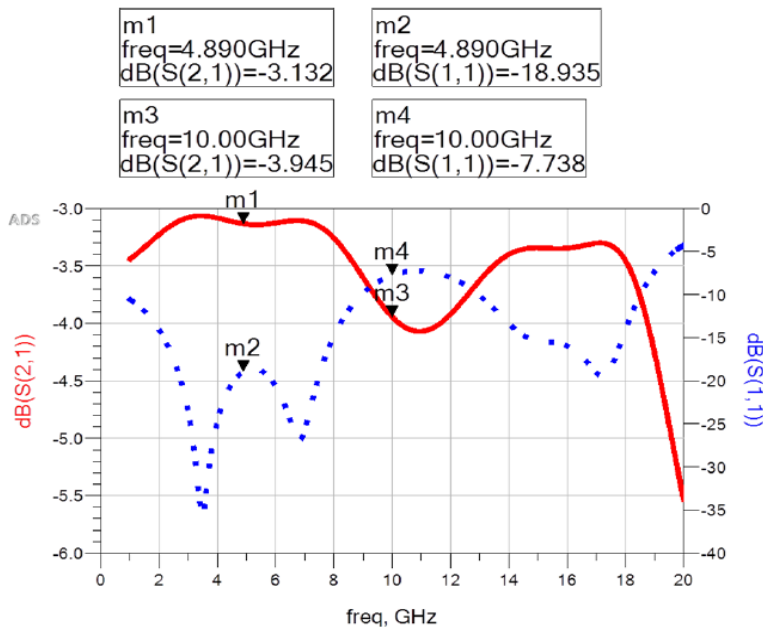


Figure 12. ADS Simulated Frequency Response

3.2 Branch Line Coupler

Analysis of generic Directional coupler or a basic 4 port Coupler [10-14] is presented below:.

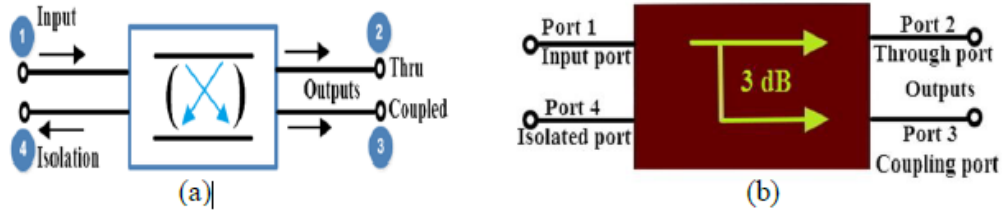


Figure 13. Portrait of 4 Port Coupler

(a). Conventional Coupler (b) Branch Line Coupler

Figure 13 depicts standard 4 port coupler while the general form of S- parameter matrix for a 4 port coupler network is given in [10] as

$$[S] = \begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} ; \quad [S] = \begin{bmatrix} 0 & \alpha & j\beta & 0 \\ \alpha & 0 & 0 & j\beta \\ j\beta & 0 & 0 & \alpha \\ 0 & j\beta & \alpha & 0 \end{bmatrix}$$

where α and β are real as they relate to magnitudes (amplitudes)

In-phase amplitude $\alpha = |S_{21}|$,

$\beta =$ Coupling coefficient $= 10^{\frac{C_{dB}}{20}} = 1.4125$ (for 3 dB coupler),

RF power conservation implies $\alpha^2 + \beta^2 = 1$

C_{dB} is Coupling value in dB given by Coupling C (dB) $= 10 \log_{10} \left(\frac{P_{in}}{P_{coupled}} \right)$ [8]; and

Coupling loss L (dB) $= 10 \log_{10} \left(\frac{P_{in}}{P_{out}} \right)$ [5] (or) $L = 10 \log_{10} \left[\frac{1}{\{1 - 10^{-(C/10)}\}} \right]$;

Coupling factor C (dB) is given as

$$C \text{ (dB)} = 10 \log \frac{P_1}{P_2} = -20 \log |S_{31}| = -20 \log \beta \quad 1$$

where amplitude $\beta = |S_{31}|$ for Quadrature (Q) or coupling port

Transmission factor or Insertion Loss is

$$IL \text{ (dB)} = 10 \log \frac{P_1}{P_2} = -20 \log |S_{21}| = -20 \log \alpha \quad 2$$

where amplitude $\alpha = |S_{21}|$ for In-phase (I) or the through output port

Isolated Port is 4, so that no power is being delivered to port 4. Isolation I (dB) is

$$I \text{ (dB)} = 10 \log \frac{P_1}{P_4} = -10 \log |S_{41}|^2 = -20 \log |S_{41}| \quad 3$$

Directivity D (dB) = (Isolation - Coupled port response) = (I - C)

$$\Rightarrow D \text{ (dB)} = 10 \log \frac{P_2}{P_4} = -20 \log \left| \frac{S_{21}}{S_{41}} \right| = [\text{dB}\{S(4,1)\} - \text{dB}\{S(3,1)\}] \quad 4$$

Phase Difference (P) between through (I) and coupled (Q) ports is

$$P \text{ (deg)} = [\text{phase}\{S(1,2)\} - \text{phase}\{S(1,3)\}] \quad 5$$

3.3 Distributed Element BLC Model using ADS

Fig.14 depicts BLC Distributed Model[8] that is being optimized in ADS to Compensate the Microstrip TEE effects Connections using ADS

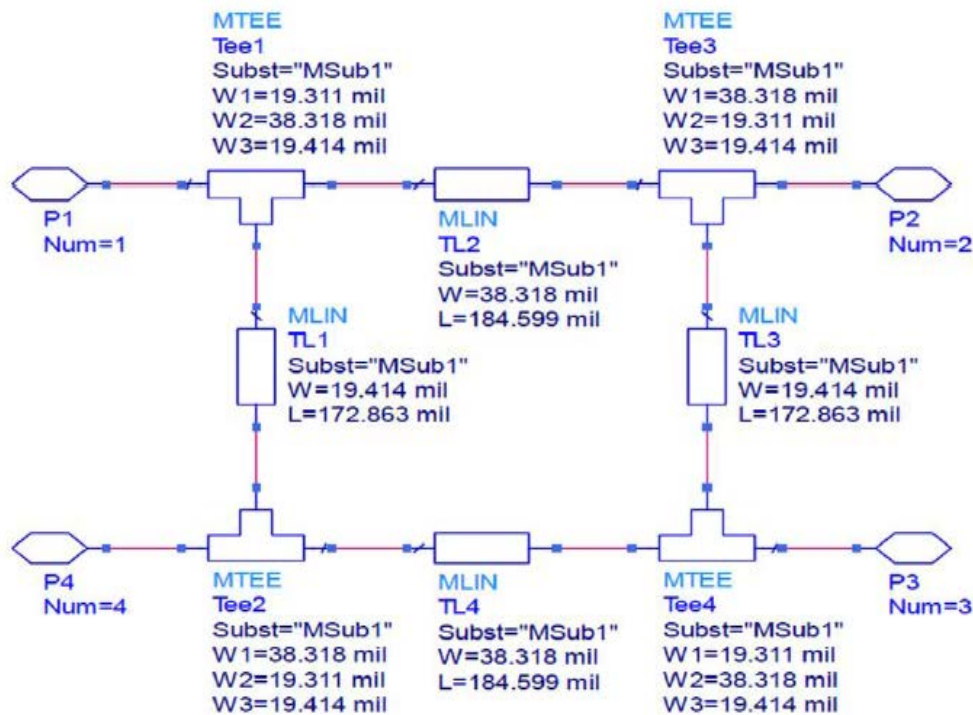


Figure 14. Schematic of BLC Distributed Element Model

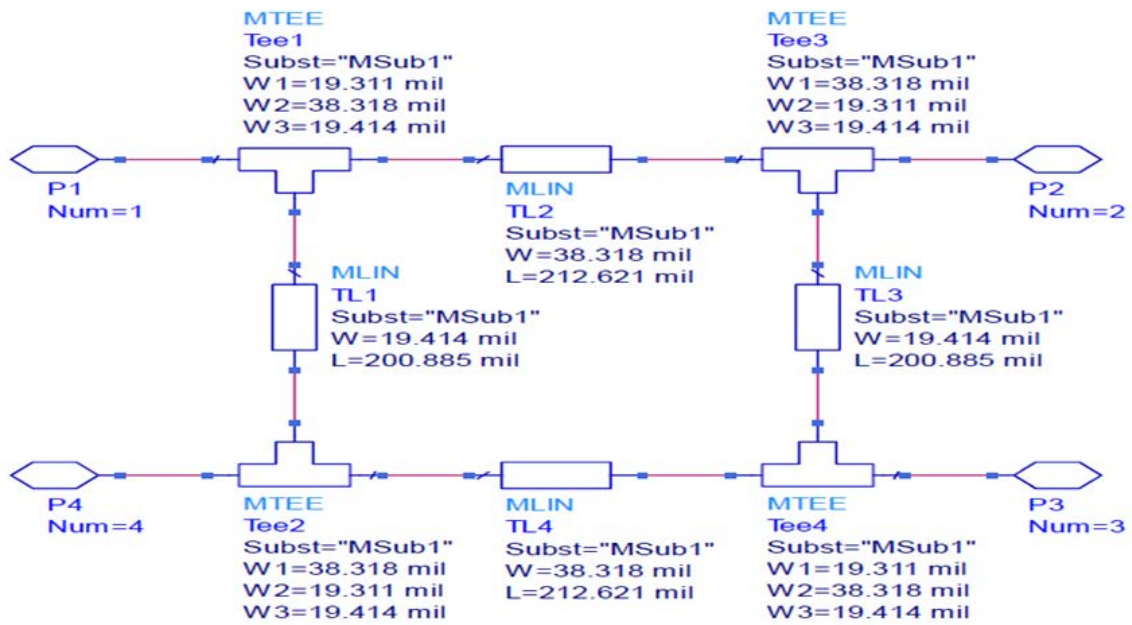


Figure 15. Schematic of Optimized BLC Distributed Element Model

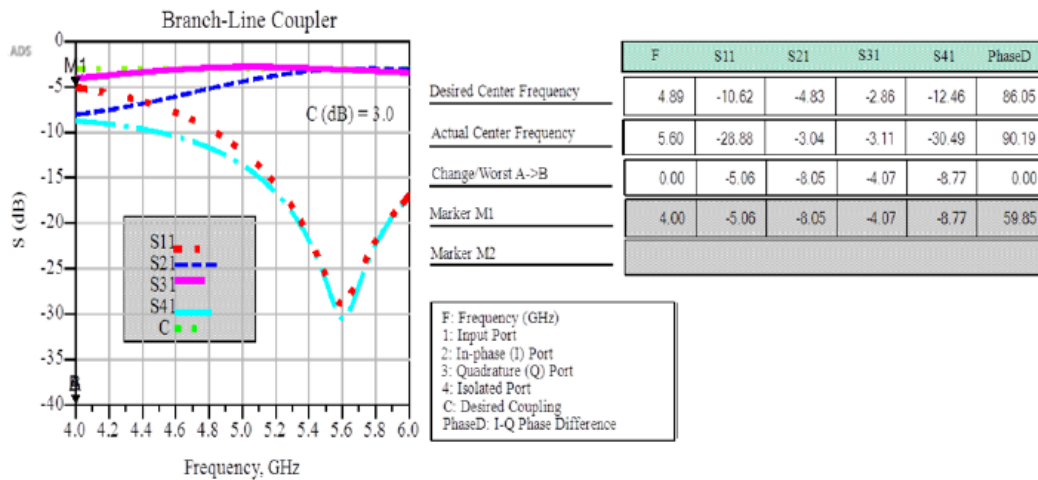


Figure 16. S-Parameters of BLC using the non-optimized smart Component Schematic

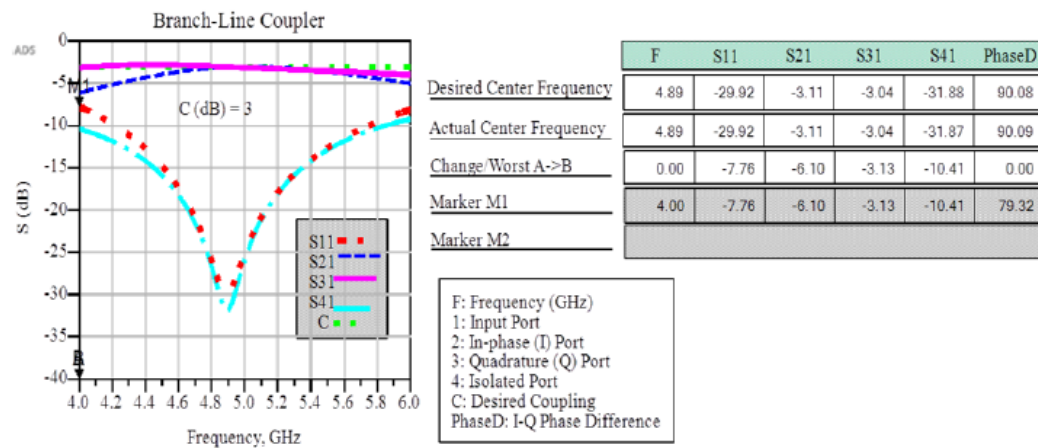


Figure 17. S-Parameters of BLC using the ADS optimized smart Component Schematic

4. Power Limiter Design with Results

Fig. 17 depicts ADS schematic while Fig. 16 provides the modeled results of the RF power limiter.

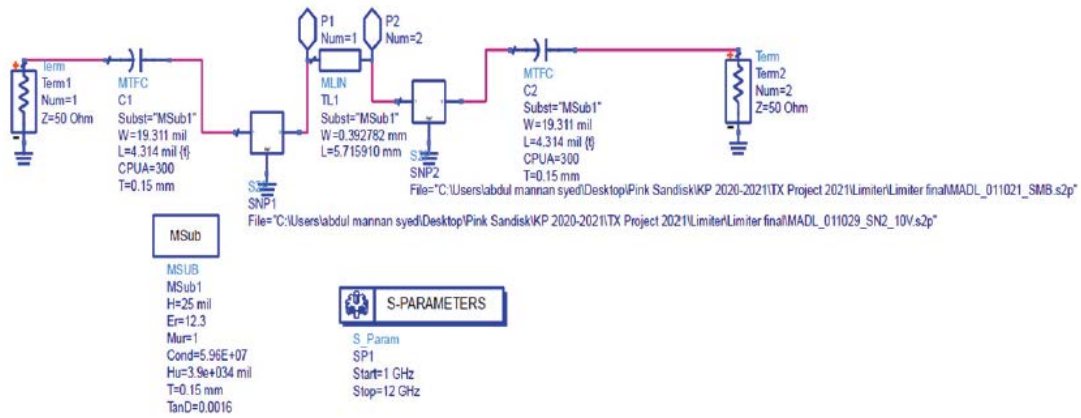


Figure 18. ADS Schematic of Power Limiter

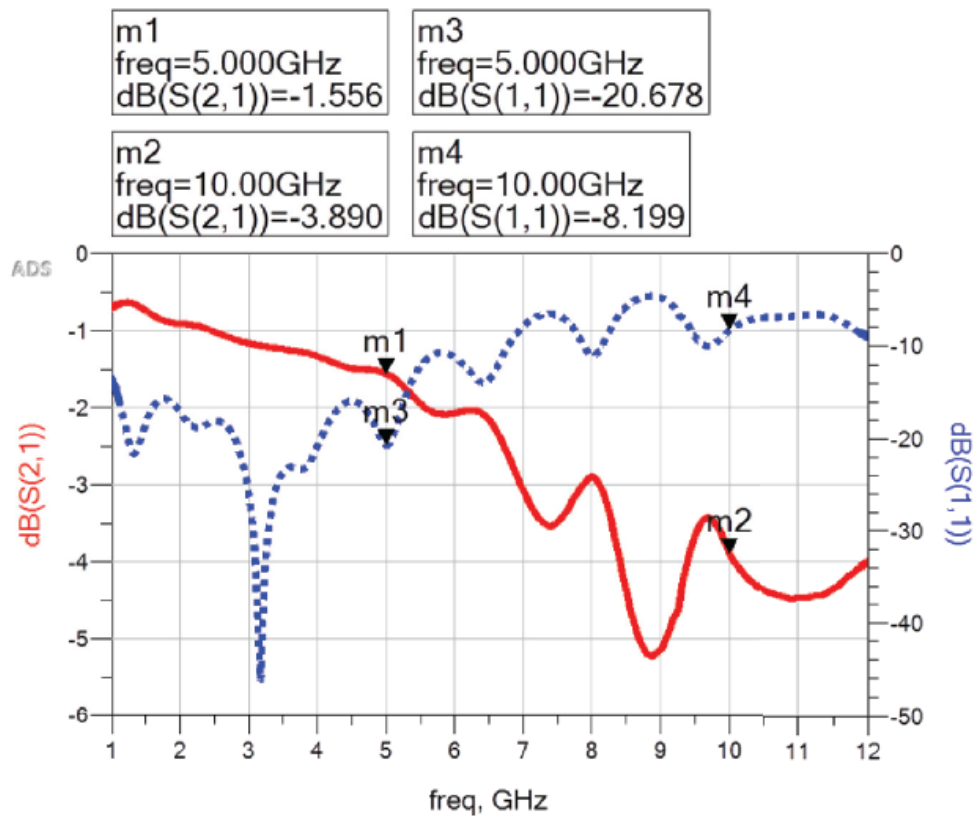


Figure 19. ADS Simulated Insertion Loss (S₂₁) and Return Loss (S₁₁)

4.1 Design of Power Amplifier

Design parameters of ADS components are being incorporated into MMIC-RFIC integrated models. These are utilized from the available standard ADS PDK library to develop ADS behavioral models and subsequently simulate the system response of RF Front End.

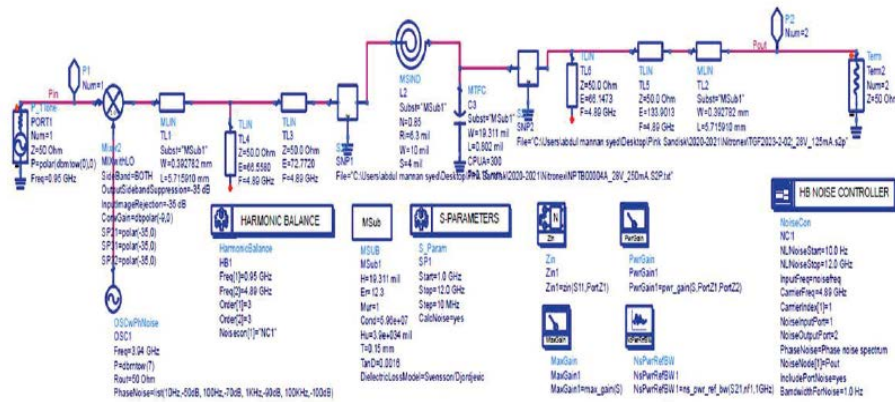


Figure 20. 1-Tone Excitation PA System Model

4.2 Results

The PA system Model Results are in Fig 21

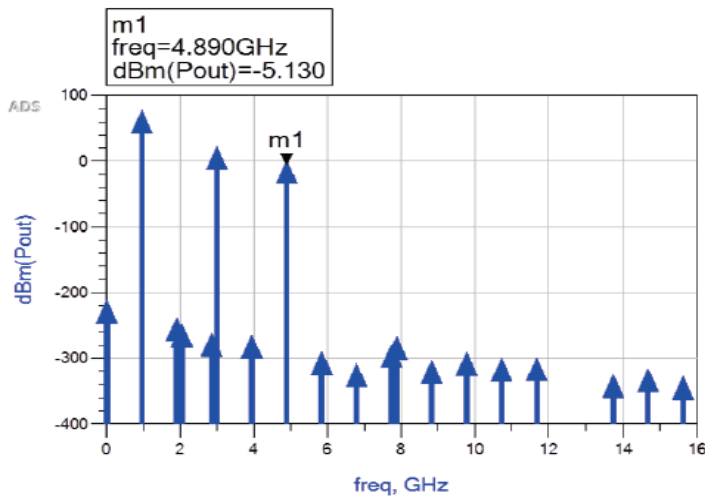


Figure 21. System Response depicting output spectrum (P_{out}) in dBm.

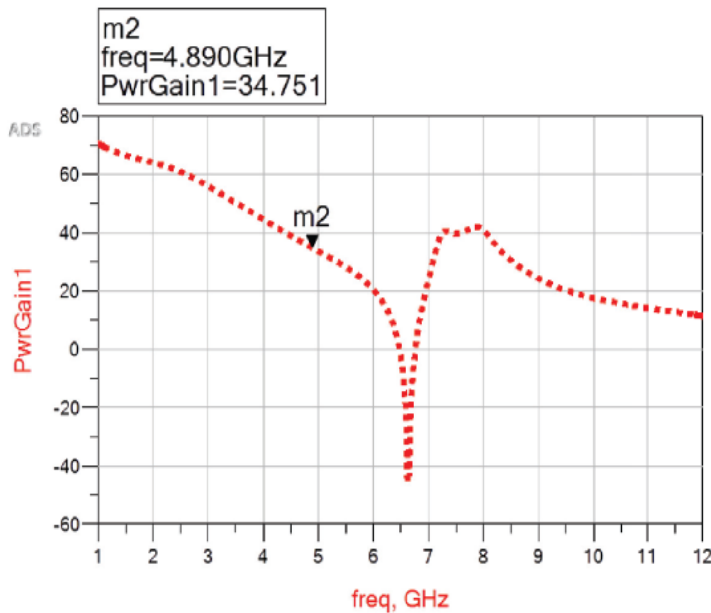


Figure 22. Power Gain (dB) simulated from 1-Tone excitation.

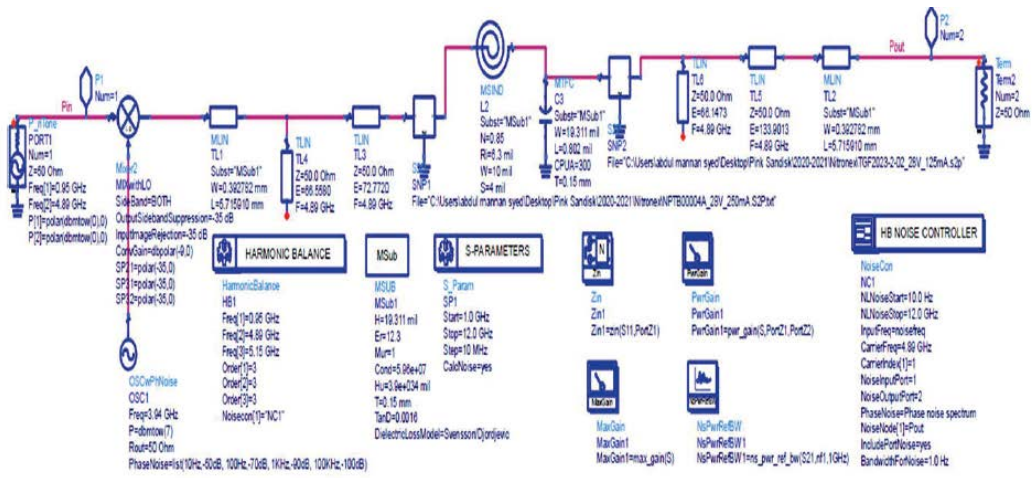


Figure 23. 2-Tone excitation PA System Model.

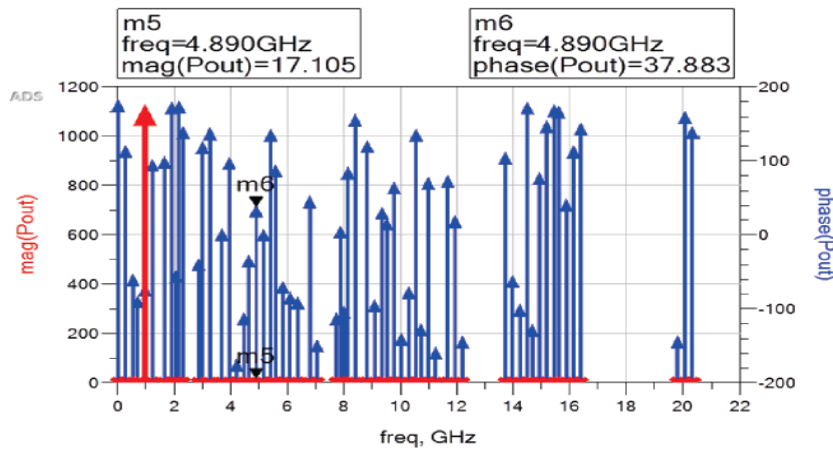


Figure 24. System Response of 2-Tone Excitation.

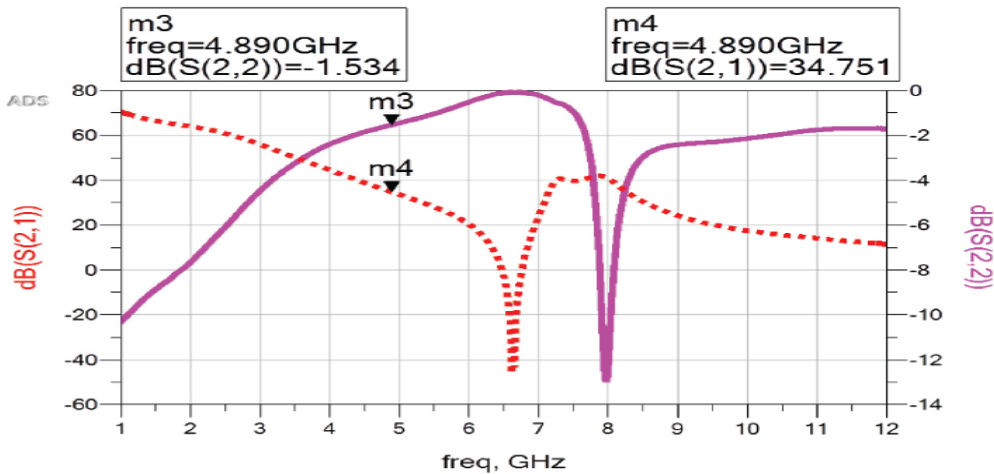


Figure 25. Frequency Responses for each of the PA System Models.

5. Microstrip Patch Antenna Design [15]

The MPAs are thin metallic conductors micro strips called “Patch” [6] placed above the ground plane separated by a dielectric substrate, whose thickness ‘t’ is much smaller than the free space wavelength ‘ λ_0 ’.

For HF applications, MPA is a MMIC design consisting of patch, ground plane, and dielectric substrate along with feeding mechanism. Usually height of substrate $h \ll \lambda_0$, and typically $0.003\lambda_0 \leq h \leq 0.05\lambda_0$. Geometry of MPA is portrayed in Fig. 26. The rectangular and square patches are the most popular types due to the ease of their design, analysis and MMIC fabrication along with their desired radiation pattern and lower polarization radiation.

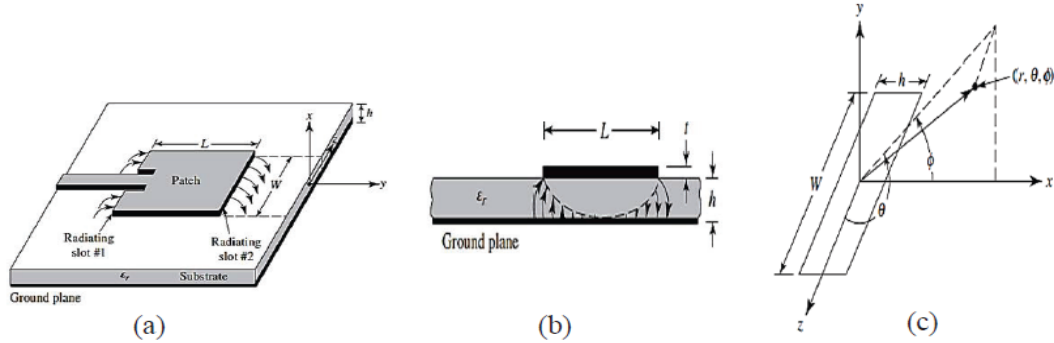


Figure 26. (a) Geometry of Microstrip Patch Antenna. (b) Side view of MPA (c) Radiating Slot Elements

5.1 Analytical Calculations of MPA Dimensions

ADS tools from Momentum-Microwave (MoM (UW) [4] suite are used to design the microstrip patch antenna working between 0.95 GHz to 12 GHz and the resonance frequency operable for this effort is good for 2.4-5 GHz range devices. The operating frequency $f_r = 4.89$ GHz. The substrate material for these simulations is GaAs comprising of a dielectric constant (relative permittivity) ϵ_r value of 12.3. The substrate height 'h' of dielectric used for design is 0.635 mm (25 mils), as this is the standard height of GaAs substrate used in MMIC designs.

The design of the rectangular patch antenna is accomplished using essential formulas from [15-19]. The rectangular patch design parameters using the geometry depicted in Fig. 26 (a) are calculated by using equations (6) through (10).

The width 'W' of the patch is obtained by:

$$W = \frac{1}{2f_r \sqrt{\mu_0 \epsilon_0}} \sqrt{\frac{2}{\epsilon_r + 1}} = \frac{v_0}{2f_r} \sqrt{\frac{2}{\epsilon_r + 1}} \quad (6)$$

Where v_0 = free space velocity of light = 3×10^{11} mm/s, f_r = Resonant frequency = 4.89 GHz, ϵ_r = GaAs-Relative Permittivity, so that from Eq. (6), Patch width 'W' = 11.895 mm ~ 12 mm.

The effective permittivity constant of microstrip antenna is calculated using the relation:

$$\epsilon_{\text{reff}} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left[1 + 12 \frac{h}{W} \right]^{-1/2} \quad (7)$$

where ϵ_{reff} = Effective dielectric constant, ϵ_r = Dielectric constant of substrate h = Height of the dielectric substrate, W = Width of the patch

Substituting the respective values in Eq. (7), we get $\epsilon_{\text{reff}} = 11.068$ Then the extension length; L is obtained by using the below equation:

$$\frac{\Delta L}{h} = 0.412 \frac{(\epsilon_{\text{reff}} + 0.3) \left(\frac{W}{h} + 0.264 \right)}{(\epsilon_{\text{reff}} - 0.258) \left(\frac{W}{h} + 0.8 \right)} \quad \boxed{8}$$

where ϵ_{reff} = Effective dielectric constant, ϵ_r = Dielectric constant of substrate h = Height of the dielectric substrate, and W = Width of the patch; Substituting the values from previous step, we get extension length ; $L = 0.26763$ mm. Finally, the actual length of the patch ' L ' is determined by:

$$L = \frac{1}{2 f_r \sqrt{\epsilon_{\text{reff}}} \sqrt{\mu_0 \epsilon_0}} - 2 \Delta L \quad \boxed{9}$$

Where f_r = Resonant frequency, ϵ_{reff} = Effective dielectric constant

μ_0, ϵ_0 = Relative Permeability ($4\pi \times 10^{-7}$ H/m) and Permittivity (8.854×10^{-12} F/m) free space respectively
 Substitution of these values gives $L = 8.685$ mm. Ground dimensions of the antenna are essential to have a finite ground plane as shown in Fig. 26 (b). The size of the ground plane is greater than the patch dimensions by Approximately six times the height of the substrate, governed by the equations given as

$$L_g = (6h + L) \text{ and } W_g = (6h + W) \quad \boxed{10}$$

Thus, length of the ground plane $L_g = 12.495$ mm ~ 12.5 mm and width of the ground plane $W_g = 15.81$ mm ~ 16 mm.

5.2 Antenna Impedance Matching Techniques for MPA Design

Exploiting MLIN, there are two predominantly used techniques for impedance matching of the antenna. They are (a). Rectangular MPA Impedance transformer matching section, and (b). Square MPA coupled with Recessed Microstrip line feed.

5.2.1 Analytical Calculations for Rectangular MPA Design

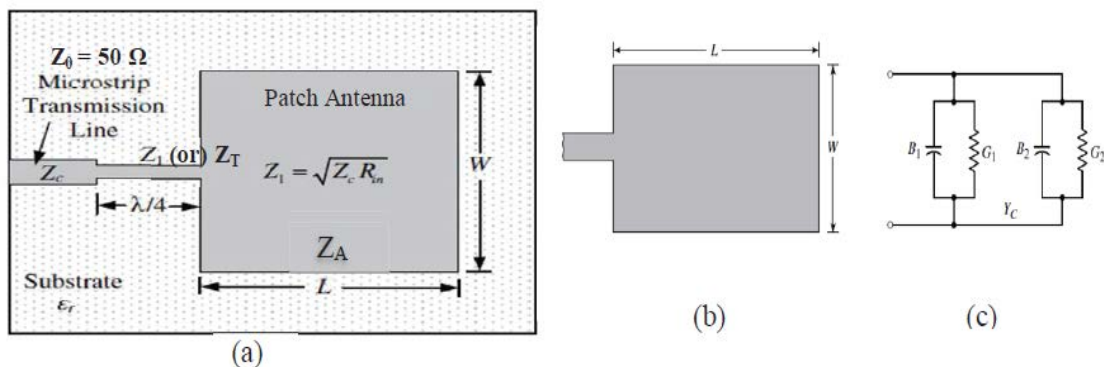


Figure 27. Microstrip patch Antenna (a) Quarter-wavelength Impedance transformer (b) Geometry Comprising of Copper center Patch feed (c) Transmission Line Model Equivalent Circuit.

For the Quarter-wavelength transformer section depicted in Fig 27(a)

$$Z_1 \text{ (or) } Z_T = \sqrt{Z_0 \cdot Z_A} = \sqrt{50 \cdot Z_A}$$

where Z_{in} = Input Impedance, Z_0 = Impedance of the transmission line with 50 Ω characteristic impedance, and Z_A = Impedance of Antenna.

The design requirement is to match Z_{in} to Z_0 value for maximum power transfer from source to the load with fixed internal impedance of source (50 Ω).

$$\Rightarrow Z_{in} = Z_0 = \frac{Z_T^2}{Z_A} \quad \boxed{11}$$

Z_{in} can be varied by selecting Z_T such that $Z_{in} = Z_0$ and the antenna will be impedance matched. By feeding the patch antenna at the end, it yields a high input impedance value of Z_{in} as current is lower at patch ends (Impedance $Z = V/I$).

Impedance of the patch is given by

$$Z_A = 90 \cdot \frac{\epsilon_{reff}^2}{(\epsilon_{reff} - 1)} \cdot \left(\frac{L}{W}\right)^2$$

With 'L' and 'W' being the patch dimensions,

$$\Rightarrow Z_A = 573 \Omega$$

$$\therefore Z_T = \sqrt{50 \cdot Z_A} = 169.26 \Omega$$

12

Ground plane dimensions from Fig. 27 (b), the Rectangular MPA are $L_g = 12.5$ mm and $W_g = 16$ mm. For the calculation of width (WT) and length (LT) of (Quarter-wavelength) transformer section having narrow strip dimensions, Eq. (13) is used.

$$Z_0 = \frac{60}{\sqrt{\epsilon_{eff}}} \ln\left(\frac{8h}{W} + \frac{W}{4h}\right) \quad \text{for } W/h \leq 1$$

13

But Z_T is to be matched with Z_0 (50 Ω) of MLIN so as to match impedance of feed line with patch. Substituting the values in Eq. (19), gives a quadratic equation for 'W_T'

$$\Rightarrow W_T^2 - 40.64W_T + 13 = 0$$

$$\therefore W_T = 0.32 \text{ mm (the larger value of } W_T = 40.32 \text{ mm is not considered)}$$

Since "T-line" is a Quarter-wavelength Impedance Transformer, its length is calculated as

$$L_T = \frac{\lambda_g}{4} = \frac{\lambda_0}{4\sqrt{\epsilon_{reff}}} = 4.61 \text{ mm, where } \lambda_0 = 61.35 \text{ mm is the free space wavelength at frequency } f_r$$

For MLIN (Microstrip Line) with $Z_0 = 50 \Omega$, dimensions $W = 0.392782$ mm, $L = 5.715910$ mm

Resulting from Matlab calculations.

5.3 Analytical Calculations of Transmission Line Matching for Square MPA Design[15,20,21]

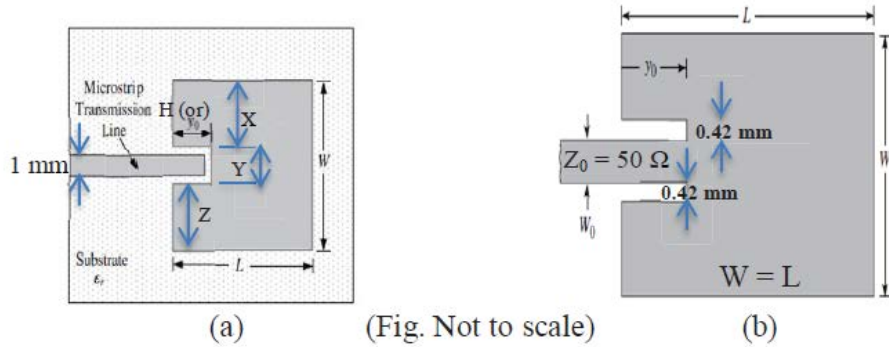


Figure 28. Microstrip Patch Antenna (a) Square Geometry comprises of Copper center Patch fed (b) Top view depicting the dimensions of Recessed Microstrip

Using Eq. (6), the Width (W) and Length (L) of the radiating surface on recessed microstrip line feed is given by $W = L = \frac{v_0}{2f_r \sqrt{\epsilon_{reff}}} \Rightarrow W = L = 9.2 \text{ mm}$

Conductor strip width of MLIN (W) = 1.666 mm (2x0.833 mm) using FEM results From [7] and $w/2 = 0.833 \text{ mm}$, so that the depth of feed line into the MPA, as illustrated in [6] is calculated as Y_0 (or) $H = 0.833 L/2 = 3.8 \text{ mm}$
Other dimensions of recessed MLIN feed in Fig 28 (a) as stated in [6]

$$Y = W/5 = 1.84 \text{ mm and } X = Z = (2W)/5 = 3.68 \text{ mm.}$$

From Eq. (10), the ground plane dimensions for Square MPA with $L = W = 9.2 \text{ mm}$ are $L_g = W_g = (6h+L) = (6h+W) = 13 \text{ mm}$.

5.4 Rectangular MPA Design with Simulation Results.

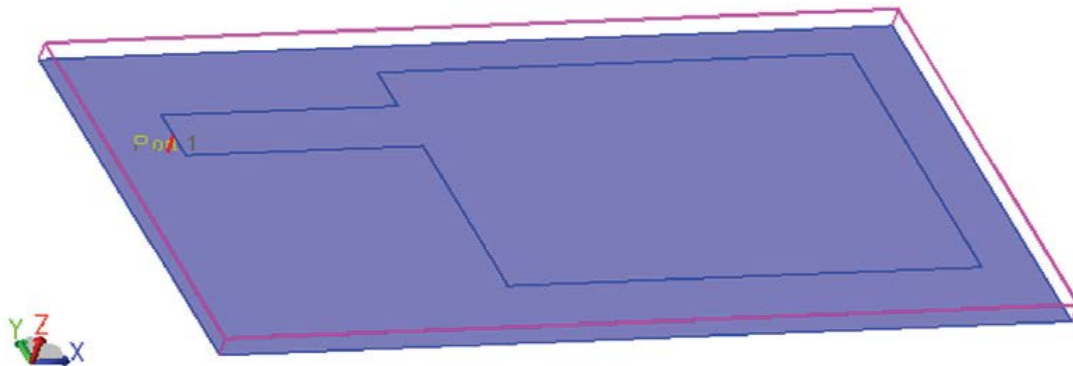


Figure 29. Rectangular Microstrip Patch Antenna

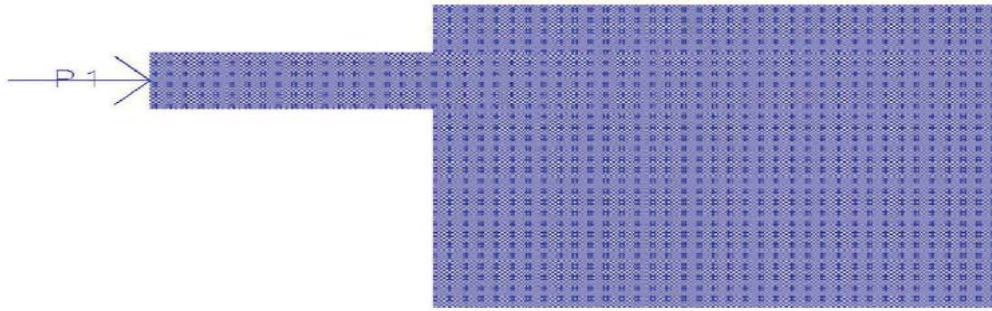


Figure 30. ADS Mesh Layout view of Microstrip Antenna

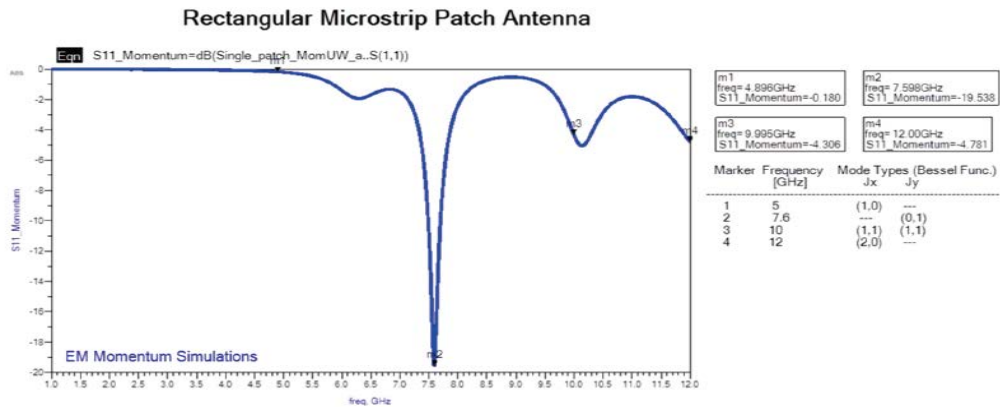


Figure 31. Return Loss S_{11} (dB) vs Frequency

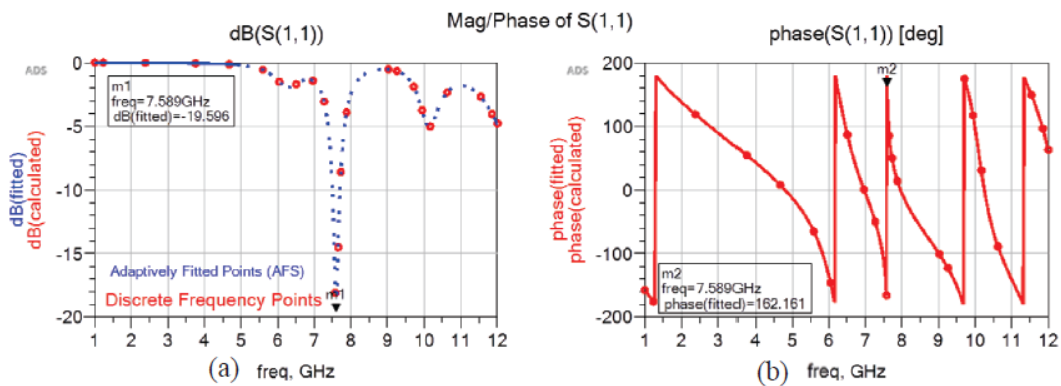


Figure 32. ADS Frequency Response (a) Magnitude Response (b) Phase Response

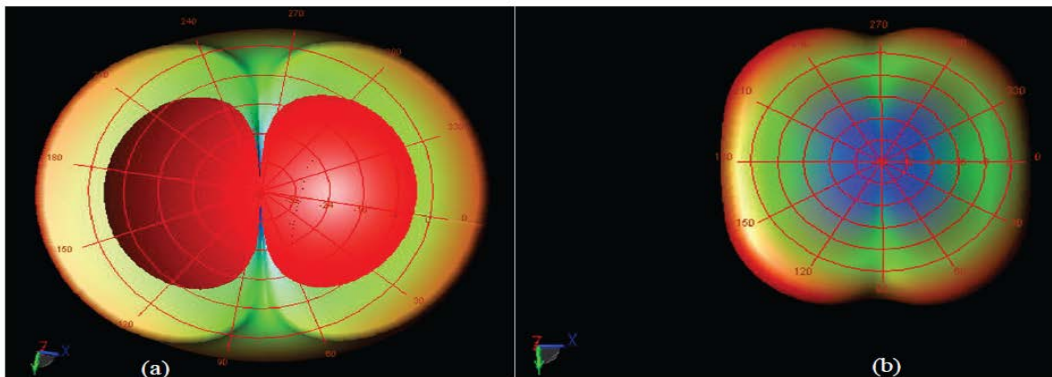


Figure 33. Far-Field Radiation intensity Patterns

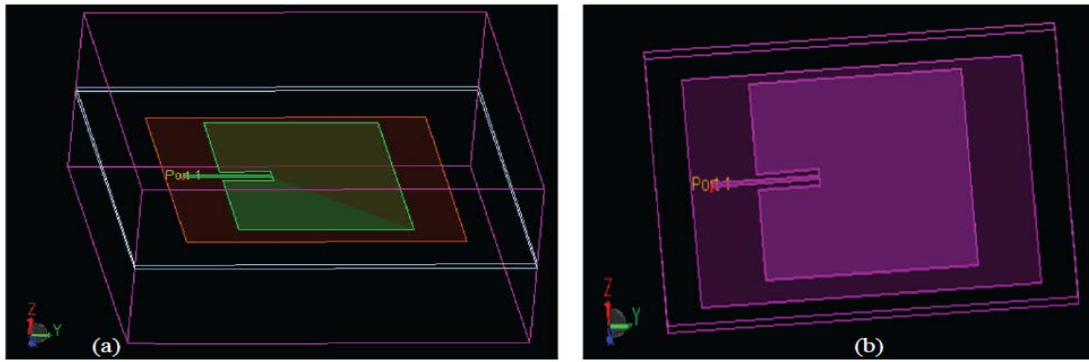


Figure 34. Single Patch 3D Isometric Schematic view of Square Microstrip Patch Antenna.

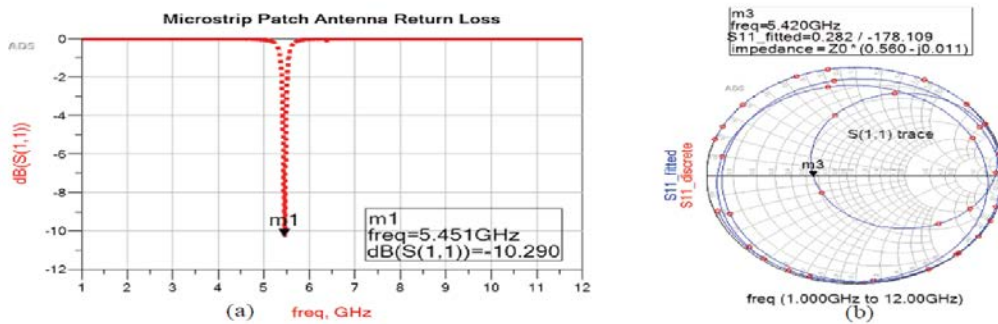


Figure 35. (a) Return Loss of S_{11} (dB) vs Frequency (b) Smith chart Quantifying MPA

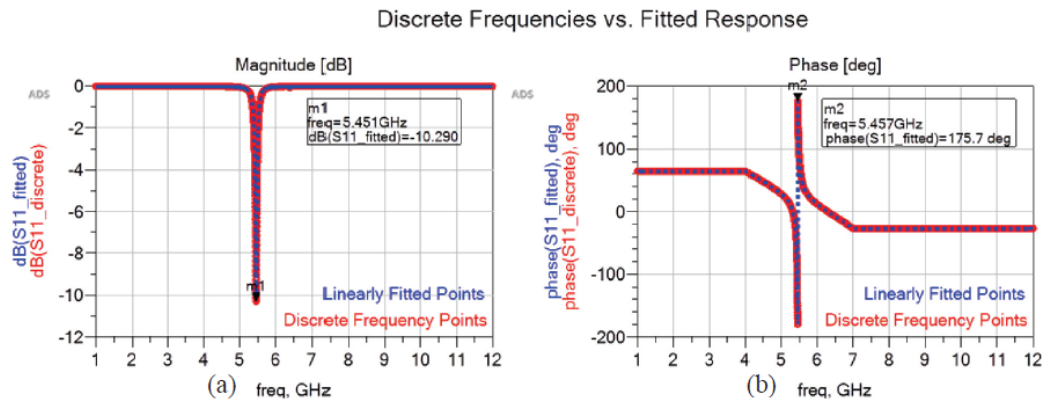


Figure 36. ADS Frequency Responses (a) Magnitude Response (b) Phase Response

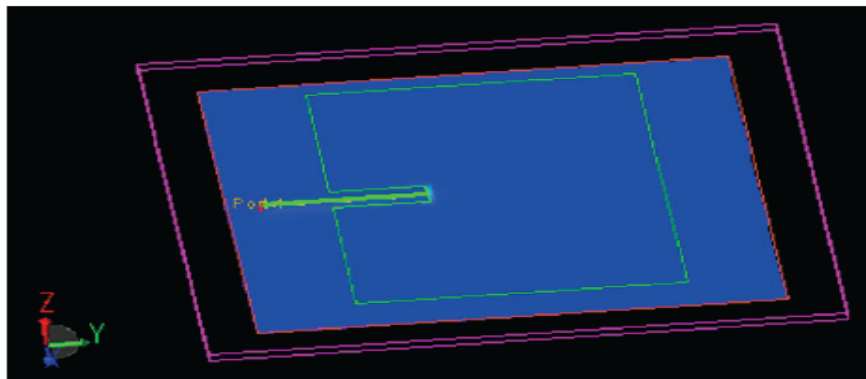


Figure 37. Visualization of electric field Strength of the MPA

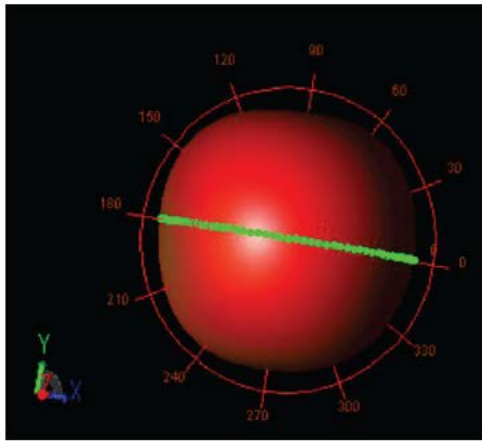


Figure 38. Post-Processed intensity Pattern of the MPA

6. CONCLUSION

RF – microwave chip-design needs multidisciplinary skills of Mathematics, Physics and Circuit Theory. To carry out device modelling precisely, the MMIC model comprised of smith chart and ECAD software (ADS) has addressed this problem adequately. An RF Engineer needs to inculcate skills in the design simulation, testing and verification along with the understanding microwave – measurements accurately. The fruitful partnership between Academia and Hi-Tech industry is of vital importance which the author has envisioned all along, especially through achieving the sponsorships for Teaching and Research endeavors in MMIC design and Fabrication activities. All the concepts of 5G chip-design have been presented in the MMIC and microwave electronics courses. Part-time students from the industry have appreciated learning a lot of fundamentals of microwave circuit design and full-time students have expressed gratitude for providing hands-on experience in the lab using ADS tools.

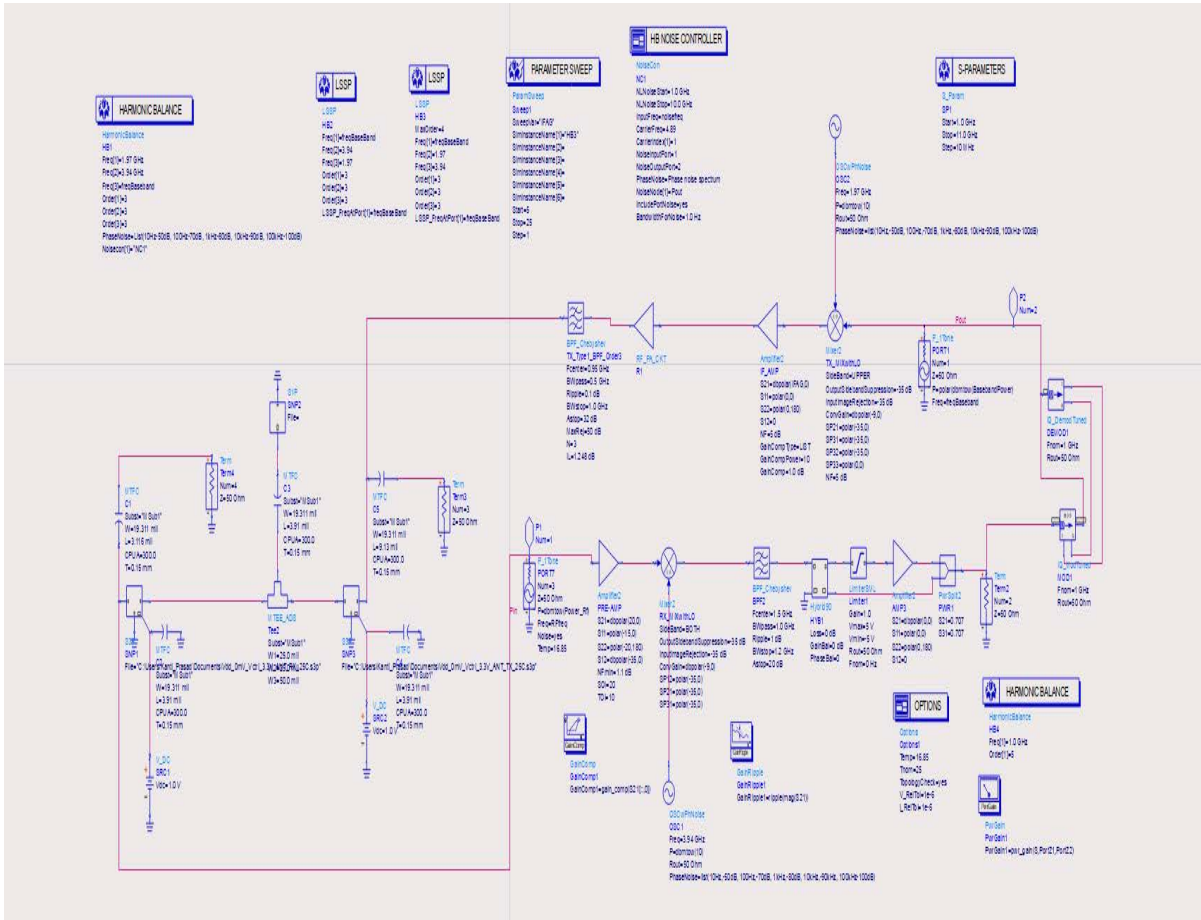
A consummate 5G chip-set has been designed as a result of teaching and research investigations. All the modules for 5G communication have been designed and simulated along with their system-level integration. There is a potential for high-end RF-PA to be able to fit the desired needs of the next generation (G) technologies including 6G communications. Presently, detailed simulations were carried out for the RF input power of 1mw (0dbm), to establish a baseline, which is the transmitter output power of 0.2W (23dbm). For future work based on the baseband expectations of 10mW(10dbm), it is to be advanced by accomplished strings standards in power analysis of RF link encompassing Front and Back-end systems for the next G wireless communications.

The author has been involved in this state-of-the-Art MMIC system level integration for the last three decades and has witnessed numerous students achieving high accomplishments in their careers.

Throughout, the mantra in the class room has been “Only those students who learned the integration of Fundamentals in Hi-Tech courses become wise, else they remain otherwise”. The earnest attempts of the author have been to place all his students into the category of the “wise”.

During these novel investigations the consummate 5G chip-set as attached has been designed simulated and is ready for fabrication.

5G Chip-Set



7. ABOUT THE AUTHOR

Dr. Kanti Prasad is an emeritus professor since 1/1/2023 in the department of Electrical and Computer Engineering and is the founding Director of Microelectronics/VLSI Technology program at UMass Lowell. He holds his Ph.D. from University of South Carolina. He is a registered Professional Engineer, P.E., in the State of Commonwealth of Massachusetts. He has been a senior member of IEEE since 1980. He is the ASEE's campus representative at the James B. Francis College of Engineering since 1992. ASEE presented the Best National Campus Representative award to him in 1999-2000 for Recruiting the Highest Percentage of New Members. He has also been awarded the Best ZONE 1 Campus Representative by ASEE 12+ times over the years for STIMULATING INTEREST AMONG FACULTY. He was Introduced in the ASEE's Academy of Fellows in 2012 based on his excellence in teaching, research, and service to the ASEE. His name is inscribed at the ASEE's Wall of Fame for Individual Membership with more than 25 years of Continuous Service, which was presented at the National Conference in 2018 held in Salt Lake City. He is promoting ASEE in India especially, recruiting deemed institutions for membership and writing a book on Circuit Theory with Applications. He has been the Graduate Semiconductor/VLSI Certificate Coordinator for the ECE Department since 1992. Dr. Prasad has developed and/or taught over 30+ Courses (List attached) at the University of Massachusetts of Lowell. He has Teaching and Industrial experience of 50+ years. He is the author of over 250 theses, dissertations and papers published and in refereed journals and/or presented in refereed conferences of national and international repute.

8. ACKNOWLEDGMENT

The author is grateful to the sponsors of teaching and research endeavors from the Hi-Tech Industry leaders and the UML Administration. Thanks are also due to Analog Devices Inc. (ADI) for supporting me in research and educational endeavors. The Author (Principal Investigator) is grateful to Ray Stata, the Co-founder of ADI for his commitment to research funds giving me motivation to carry out the investigations in integrated 5G chip design towards cutting-edge MMIC technology. Thanks are also due to Susan Puryear, Executive Director – Office of Research Administration (ORA) for her active role in getting this award to the UML. I thank Syed (my Post-Doc.) for assisting me in the design and exhaustive simulations of consummate Chipset for Mobile Communications. I also thank my student assistants Divyaksh, Achintya, Gaurav and Kaushik for typing and arranging the manuscript. Lastly thanks are also due to my beloved wife (Uma Rani Goel) for being patient with me throughout these Research Endeavors.

9. List of Courses

Offered in Chronological Order

Fall '82	16.207	Fortran Programming (Team taught with Prof. Emeritus Jim Powers)
Fall '82	16.562	Microprogramming
Fall '82	16.365	Electronics I
Spring '83	16.564	Operating Systems
Spring '83	16.366	Electronics II
Fall '83	16.561	Computer Organization
Fall '83	16.311	Electronics I Lab
Spring '84	16.312	Electronics II Lab
Spring '84	16.502/469	VLSI Design
Fall '84	91.454	PC Design
Fall '85	16.661	Local/Computer Area Network
Spring '87	16.504/470	VLSI Fabrication
Spring '90	16.602	Advanced VLSI Design
Fall '94	16.419	Introduction to ITS Technologies
Fall '94	16.753	Ph.D. Dissertation
Fall '96	ENGIN292	Digital System Design (at UMass Boston)
Spring '97	16.710	Directed Study
Sum. '97	16.733	Advanced Graduate Project
Spring '98	16.602	VHDL Based Digital Design
Spring '98	16.517	MMIC Design & Fabrication

Fall '00	16.210	Semiconductor Basics (at ADI)
Spring '01	16.265	Logic Design
Sum. '01	16.743	M.S. Thesis
Spring '02	16.400	Engineering Topics
Fall '02	16.399	Capstone Proposal
Fall '04	16.202	Circuit Theory II
Fall '05	16.201	Circuit Theory I
Fall '06	16.211	Fundamentals of Electricity
Fall '06	16.213	Fundamentals of Electricity
Spring '19	EECE.5050	Microwave Electronics

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