DEVELOPMENT OF A TMS320C30 DSP BASED CONTROLLER FOR A POWER CONVERTER

S.A. Chickamenahalli, Rutledge Ellis
Wayne State University/Visteon

Abstract:

This paper presents an undergraduate research project that involved the design, development, testing and installation of a DSP based controller for a power converter. The parallel interface for a Texas Instruments TMS320C30 Digital Signal Processor (DSP) established to devise an economical real-time interface is discussed. Derivation of signals for the power devices of a single-phase topology of the power converter, with expansion capabilities for a three-phase configuration is detailed. The advantages of C programming capabilities of the DSP are highlighted. Experimental results are presented and the scope of future work is summarized along with conclusions.

I. INTRODUCTION

The scope of applications of digital signal processors (DSP) has increased steadily over the last few years. R. Chassing et.al [1, 2] and J. Maisel [3] describe some of the traditional communication applications for which DSP's were originally meant. However, due to their capability to handle complex tasks numerically, there have been several applications of DSP's in Power Electronics [4-6]. Lately realized is the C programming capabilities of the DSP which enable user freedom from tackling assembly language instructions. There has been an increasing interest in courses in digital signal processing in engineering technology curricula. The exploration of projects based on DSP's requires knowledge of both hardware and software from the student who intends to accomplish the goals of a project on time. The basic background required is in digital logic, a/d and d/a conversion, and assembly and / or C language programming skills.

This paper addresses a power electronic application [7-8] built around the capabilities of a TI DSP. Although the current project utilizes the fixed-point capabilities, the floating-point capabilities are being explored in an ongoing project to control the torque characteristics of a three-phase induction motor. Many of the communication applications utilize the DSP's serial ports for interfacing. The controller description in this paper includes the development of the parallel interface, as the serial port interface is only applicable for a limited number of signals. An Intel 8255 parallel peripheral device was adopted for the interface. The hardware consisted of address generation and buffering circuitry. To accomplish the interface, a C language program that contained the information on the timing sequences of the devices of the power converter was developed.

II. CONVERTER CONFIGURATION

A single-phase circuit of the converter used for interfacing along with the controller is shown in Figure 1. The input bridge is an ac to dc pulse width modulated (PWM) rectifier. The output bridge is a dc to ac PWM inverter. Both bridges are current controlled. The link is resonant commutated to achieve minimum switching losses in the system. The converter is capable of producing variable currents at variable frequencies that can be utilized to control an ac motor. It is modeled as a two-port network that can allow bi-directional or zero current flow at one port independent of the conditions at the other port. The eleven power devices (SCR's) of the converter are given triggering signals in a predetermined manner from the controller. A fixed frequency, fixed input voltage converted to dc by the input rectifier bridge is converted to ac by means of the output bridge or the inverter at a desired frequency. The duration of device cycles in the input and output bridges is independently controllable by software. The devices and the resonant components of the link L_{01}, L_{02} and C_0 provide for the resonant commutation of the link and the recharging of the commutation capacitor C_0 with which switching losses in the system are minimized [7]. The potential applications of this converter are adjustable speed drives including electric vehicle drives, welding, static var compensation, and active filtering.

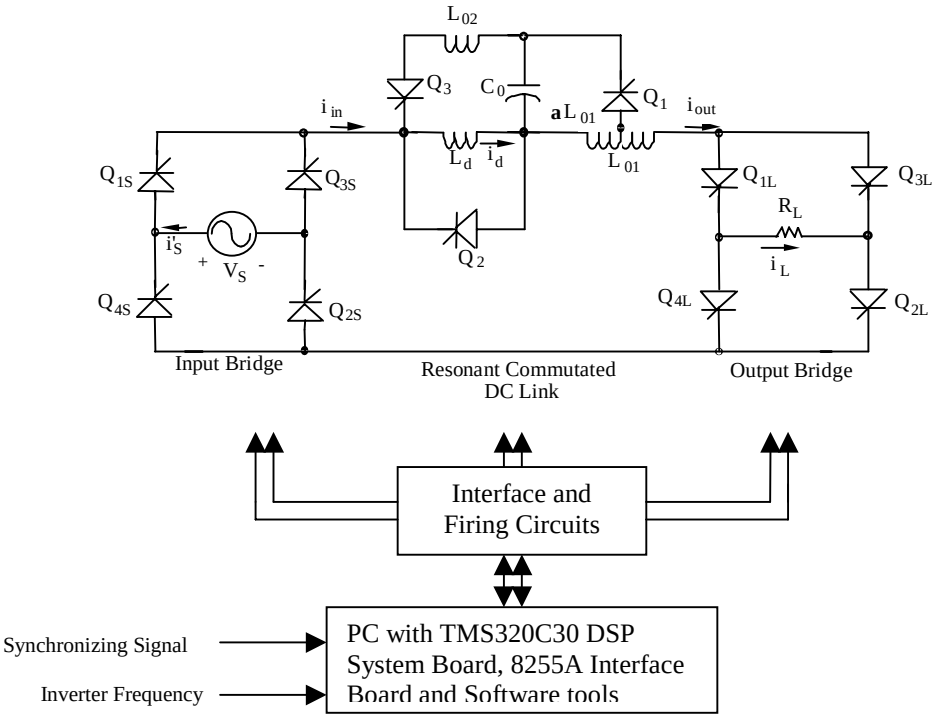


Figure 1. Circuit schematic of the single-phase system

III. CONTROLLER CONFIGURATION

A 486 IBM PC housed a System Board [9] consisting of: a) the Digital Signal Processor (DSP), b) Two Analog-to-Digital converters, c) Two Digital-to-Analog converters, d) Associated circuitry to enable memory, parallel, and serial bus expansions along with the software tools

form the main controller components. The DSP used is the Texas Instruments TMS320C30, a 33 MHz, 40 pin, floating-point type digital signal processor. Software tools included a TI TMS320C30 C compiler, assembler and linker, and a Spectrum Signal Processing source debugger. The program was complied and linked using the C compiler and linker of the DSP. The program outputs Sinusoidal Pulse Width Modulation (SPWM) [7] signals for both the source and load, and link devices of the converter. Three pulses per half cycle were utilized in the first stage of testing. The digital outputs obtained from the parallel ports were interfaced with the power circuit through stages of isolation, amplification and gate driving circuitry to bring up the switching action of the SCRs.

(a) Controller design and development

The essential steps involved in the design and development of the controller were:

(i) Building of Control circuit
  (a) Development of the algorithm to derive the converter device switching patterns
  (b) Programming of the DSP to address DSPLINK and 8255 PPI
(ii) Testing to insure DSPLINK - 8255A interface and converter operation

Traditional DSP serial ports are configured in Transmit/Receive model. However, this application [8] used the serial port (0 and 1) register lines in general input/output mode. This consisted of elaborate outputting to the serial port registers in order to produce the required signals for the single-phase converter devices. To eliminate this procedure and provide future expansion to three-phase signal generation, Parallel Expansion (DSPLINK) was planned [10].

The DSPLINK is a high-speed bi-directional bus that allows input/output directly to/from the DSP. The signals available to the DSPLINK connector from the DSP were data lines D15 - D31, address lines A_0 - A_{12}, Reset, and Write, In/out enable (/IOEN). To achieve the interface, an Intel 8255A-Programmable Peripheral Interface (PPI) device was used [11]. The different modes of the 8255A were studied, and configuration of Mode 0, which produces twenty-four outputs, eight each from ports A, B, and C was chosen. For the single-phase converter, ten pulses were needed, four each for input and output and two for the DC Link with two of the three switches fired simultaneously. Therefore Port C was not used. The control word that initialized the 8255A for the required mode was 80 H (or binary 10000000). However, the word 80 H had to be changed to 80,0000 H in the trial program because of the DSP's Most Significant Bits'(MSB) termination only on the DSPLINK.

Once the type of operation of the 8255A was known, the hardware had to be built in order to support that operation. As a programmable device, the 8255A needed addressing in order to receive the control word and direct data to ports A, B and C under programmable control. A TTL 3 to 8 decoder 74HC138A was used to derive the /Chip Select for the PPI device, with address lines A_2-A_4 of the DSPLINK as inputs. The state of the address lines determined the mode of operation. The decoder output Y7 was taken to the /Chip Select of the 8255A whereas A_0 and A_1 were connected directly to its A_0 and A_1. With A_2-A_4, and /Read held at binary 1's and /Write and /Chip Select held at binary 0's, the only control of the 8255A is by the state of the address lines A_0 and A_1. Thus address bits were 11111 (1F H), in the order of A_4,

A_3, A_2, A_1, and A_0 respectively. Address lines A_5 -A_7 were not used.

The memory expansion of the system board required the DSPLINK initialization at 80,0000 H. Any peripheral device configuration must take this address into account. In order to direct the control word of 80,0000 H to the 8255A, the control mode obtained above with A_1A_2 = 11 and /Chip Select (/CS) enabled with $A_4A_3A_2$ = 111 amounted to the address DSPLINK+ $A_4A_3A_2A_1A_0$ = 80001F H for the control word. With A_0 and A_1 taking the four possible states and A_2-A_4 being 111, the addresses of the control word, Ports A, B, and C, were 80001F, 80001C, 80001D and 80001E respectively.

The DSPLINK provided only a /Write output. The PPI device required both /Read and /Write inputs. Hence a 74LS04 Inverter was used to invert the /Write signal to provide the /Read input. The Reset available on the DSPLINK is an inverted signal. It was inverted, and connected to the 8255A. The 74LS17 hex buffers for the data lines were replaced by octal buffer/drivers 74LS241 later in order to strengthen and achieve distinct output signals. The outputs of the buffers were tied to their respective inputs on the PPI device. An external 5V-power supply was provided to supply all the external devices.

(b) Controller testing

The trial program was made ready by shifting all data to the most significant bits in order for the DSPLINK to recognize the information. This entailed putting zeros for the 16 least significant bits. The DSPLINK was sixteen bits wide and the 8255A is an eight-bit device. In order to direct desired data to ports A and B of the 8255A, two consecutive outputs from the DSPLINK were required. Also found was the fact that the access time of the DSPLINK for sustained data required the data to remain on the bus, for a certain length of time. Hence a for-loop in the output statement enabled meaningful data output to the DSPLINK.

Once the trial program was ready, testing of the prototype circuit board was possible. The final circuit consisted of the 8255A, 74HC138AP Decoder, 74LS04N Inverter, outputs of the DSPLINK, and two 74LS241 Octal buffers, all components placed on a wire wrapped circuit board. Figure 2 shows a connection diagram of the interface circuit. The output of the modified circuit met all of the system specifications. The board was successfully tested which established the PPI. Several tests were conducted to ascertain various aspects of the DSPLINK. When all aspects of the board and trial program were tested, the modified board was redesigned and built in order that it can be housed in one of the PC slots. The new board operated successfully. When the trial program produced the desired results from Ports A and B, the data was changed in order to produce the actual outputs required for the devices in the single-phase converter circuit. Figure 3 shows the switching signals at the 8255 output for the case of fixed frequency at the source and load. Figure 4 shows the load voltage waveform for a passive load, which signifies the PWM operation of the converter as demanded through the controller signals. Currently the board is functional in a three-phase motor drive controller configuration.

IV. STUDENT ROLE AND EDUCATIONAL VALUE

The student began this research by reviewing the previous work done on the project. He won a grant under the NSF funded Alliance for Minority Participation program at the university for his project

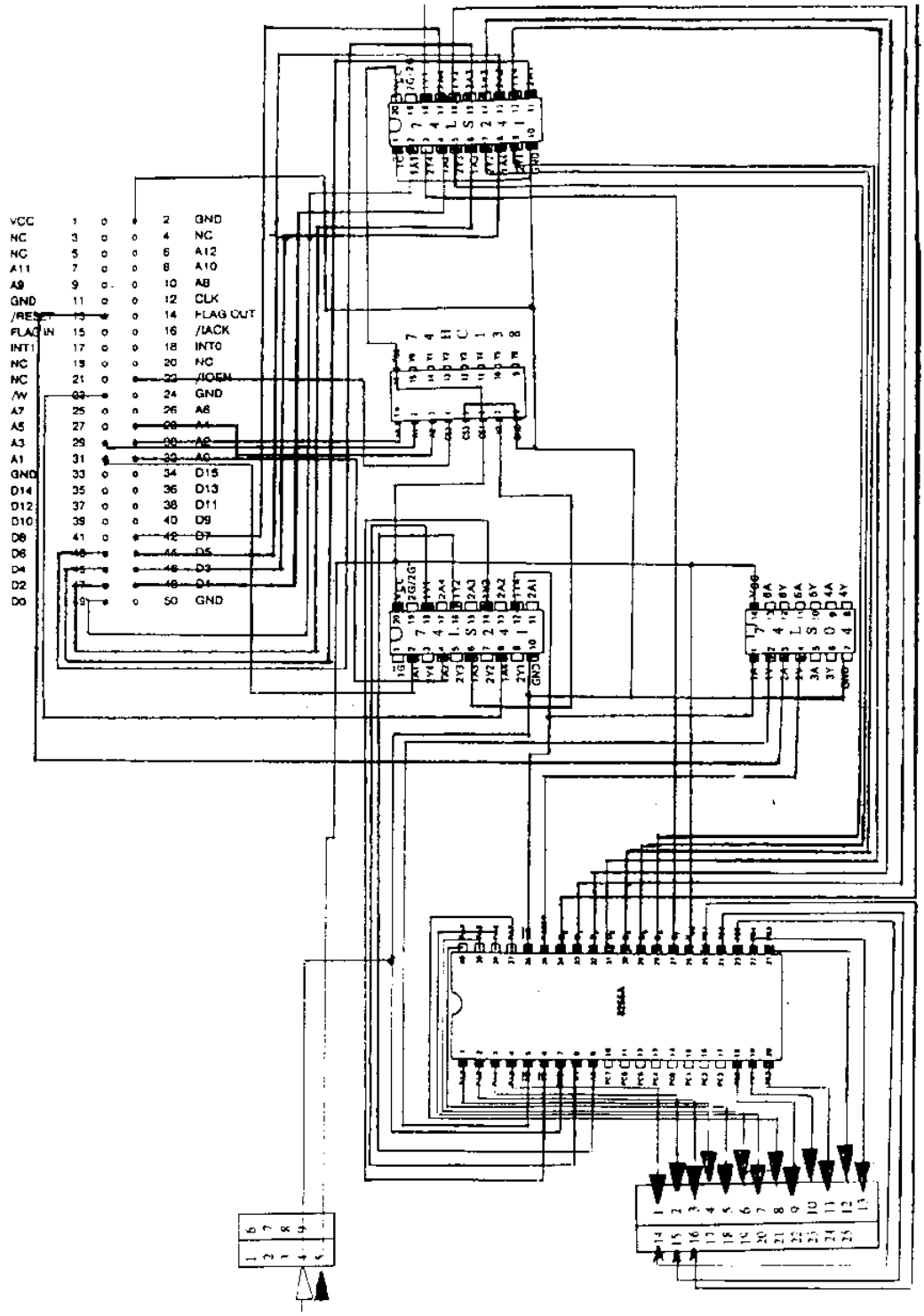
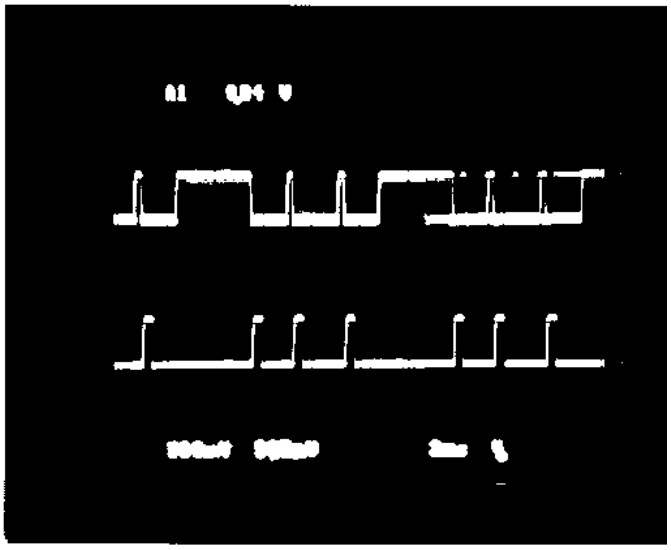
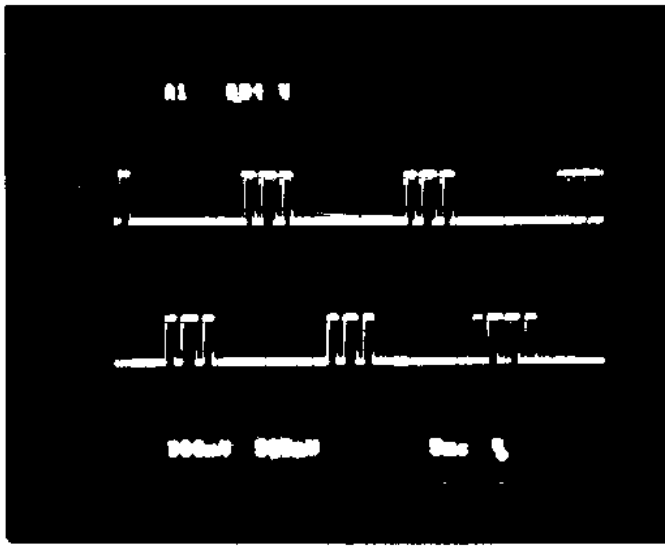


Figure 2. Parallel interface connection diagram



3(a)



3(b)

Figure 3. Switching signals for different converter devices (a). Signals for Q_1, Q_2 (top trace) and Q_3 (bottom trace). (b). Signals for Q_{1S}, Q_{2S}(Q_{1L}, Q_{2L}) (top trace)and Q_{3S}, Q_{4S}(Q_{3L}, Q_{4L}) (bottom trace)

proposal to begin with. The student designed, built, installed and tested the Parallel Interface of the DSP. Other students currently utilize this interface board in the signal generation stage for three-phase operation. He also assisted in modifying and running the DSP C programs and was mainly

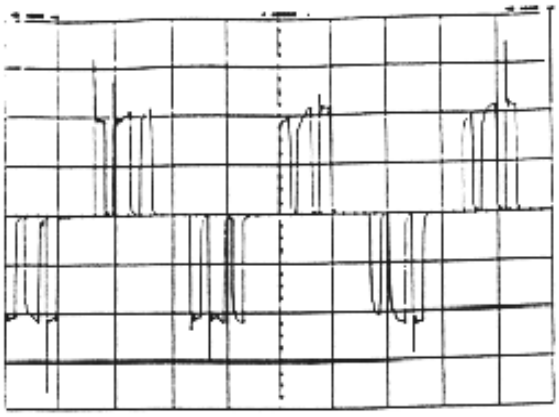


Fig.4. Output voltage waveform with passive load

responsible for all the findings that lead to the success of this work. The student efficiently utilized the Internet for technical literature and effectively collaborated with other graduate students and the technical support personnel at Spectrum Signal Processing while working towards the goals of this project. The successful pattern set forth by this student has been followed by several of his teammates later last year in securing funding for their research project, and in effectively utilizing their technical education to accomplish the set goals of their projects. Projects of this kind fit to fulfill the senior project requirements in the division on a regular basis. Hardware, software, troubleshooting and mixed mode simulation expertise attained by the student has proved beneficial not only academically but also commercially.

V. CONCLUSION AND SCOPE OF FUTURE WORK

A parallel peripheral interface to a TMS320C30 DSP was designed, built, installed and tested. To establish the interface, an Intel 8255A PPI and the Parallel data bus termination (DSPLINK) of the TMS320C30 DSP System Board were utilized. The interface enabled generation of more number of signals than those derivable with the serial port interface. The developed interface is currently adopted in an ongoing three-phase converter controller development. The project enabled a senior undergraduate electrical engineering technology student to fulfill the requirements of his bachelor's degree.

VI. REFERENCES

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SHAMALA CHICKAMENAHALLI

Shamala Chickamenahalli is an assistant professor in the College of Engineering at Wayne State University since 1994. She earned her B.E. degree in 1984, M. Tech degree in 1986, and Ph.D. in 1995, all in Electrical Engineering. She worked in industry for five years. Her interests include power electronics and digital control, teaching and learning pedagogy. Dr. Chickamenahalli is a member of IEEE, ASEE, Tau Alpha Pi, and POET.

RUTLEDGE ELLIS III.

Rutledge Ellis graduated with his bachelor of Electrical Engineering Technology from Wayne State University in May 1997. Prior to this, he worked for more than twenty years in the U. S. military. He is currently working as an engineer at Ford Motor Company. His areas of interest include Microprocessor control, Analog electronics, and Control systems. He is a member of the Professional Order of Engineering Technology(POET).