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DIGITAL LABORATORY ENHANCEMENT

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Abstract

This paper describes the implementation of a digital laboratory enhancement using Altera's state-of-the-art laboratory equipment at Wayne State University (WSU). The unique collaboration among the WSU, the Altera Corporation and the National Science Foundation in improving the undergraduate education in the United States is explained.

I. Introduction

The profound advances we have experienced in computer technology during the last decade have propelled the need to educate every undergraduate student with the latest enhancements in technology to the forefront of educational objectives. To address this need, the digital laboratory facilities of the Engineering Technology (ET) program at WSU has received funding from the National Science Foundation (NSF) and the Altera Corporation. The objective of this enhancement project is to enrich the quality of undergraduate digital laboratory instruction by providing an environment to conduct learning about, and use of, Programmable Logic Devices (PLD), a key advance in digital electronics [1,2].

Most modern digital designs require the use of computer-aided design methods and tools. Many PLD packages today come with a simulation option where the simulation package tests the logical operation and internal timing. This allows each student to model his/her circuit design before programming it into a chip. Altera Corporation's Max+Plus II design package is used in our digital design and computer architecture classes [3]. It offers a variety of logic design capabilities which foster greater student learning. Students can combine text, graphic, and waveform design entry methods while creating their own designs. Altera's development package drastically reduces the wiring difficulties in the realization phase and enhances our students' learning about design with state-of-the-art equipment.

In this paper, the implementation of a digital laboratory enhancement and its impact on ET education at WSU is presented.

II. Methodology

Within the Electrical/Electronic Engineering Technology (EET) program at WSU, this project makes its greatest impact in the development and design of digital systems. Digital circuits are employed in the design of systems such as digital computers, data communications, and many other applications that require electronic digital hardware. The courses that are currently offered in this area at WSU are EET 2100 *Principles of Digital Design*, EET 3100 *Digital Design*, EET 4100 *Microcomputer Hardware Design*, and ET 4999 *Senior Project*.

Prior to the enhancement of this digital laboratory, the experiments in these courses were performed with traditional bread-boarding using commercially available standard integrated circuits (ICs) of the TTL type. In this context, the laboratory usually involved the construction of digital circuit with standard TTL small-scale integrated (SSI) and medium-scale integrated (MSI) circuit modules on a printed breadboard. This process however is, by its very nature, prone to wiring errors. The use of many different ICs tends to create massive interconnecting wires. It is very difficult to visually trace the path of a wire in a circuit. Most modern digital circuit designs require the use of computer-aided design methods and tools. One such tool is the Programmable Logic Devices (PLDs). PLDs are digital logic chips containing circuitry that can be *programmed* by a student to realize logic functions. In using these devices, the probability of error shifts from wiring to programming. Many PLD packages today come with a simulation option where the simulation package tests the logical operation and internal timing. This allows the students to model their circuit design before programming them into a device (an IC chip). More recently, complex programmable logic devices (CPLDs) are one of the most significant new advances in digital electronics, as they allow the student to overwrite his/her design onto the same chip, Electrically Erasable Programmable Read Only Memory (EEPROM).

We have applied for, and were awarded, the ALTERA Corporation's Higher Educational Assistance Program grant through which we received, free of charge, a number of "design laboratory packages" which included ALTERA Development Tools including a programming unit for each package. Through this program, ALTERA provides qualified institutions with development tools which support system-level digital logic design utilizing ALTERA's PLD solutions. This program serves two purposes:

(1) it enables member universities to keep pace with the latest technological advances; and
(2) through its role as an information clearinghouse, ALTERA facilitates the exchange of ideas and experiences among participating universities.

Through an NSF-ILI grant, we received Gateway Computers, one laser printer and the necessary networking equipment. Altera Corporation has donated a "Design Laboratory Package (DLP)" for each station, and a number of MAX+PLUS IIs as a professional package. MAX+PLUS II has in integrated design flow and intuitive graphical interface. It supports many features such as schematic capture, and design compilation and

verification with full timing simulation. We have implemented this hardware in our curriculum and created a user manual for our students. It contains instructions on how to use the graphical editor, how to compile and simulate their project. Altera Corp. makes available a student version CD-ROM for each student, so students can perform the simulations at home. The hardware implementation is done in the ET laboratory at WSU. The web site is http://ozric.eng.wayne.edu/~altera. In this paper, however, we show the hardware implementation methodology of our project.

III. Hardware Implementation

We have implemented the digital laboratory using the DLPs. Each DLP contains the UP1 Education Board, and with its simple design, provides an excellent environment for learning digital logic design. The University Program (UP1) Education board consists of two devices:

- the EPM7128S device
- the EPF10K20 device

The EPM7128S device is a mid-density member of the high-density, high performance MAX7000S family. The device comes in an 84-pin plastic J-lead chip carrier (PLCC) package. It has 128 logic cells that have a programmable-AND/fixed-OR array, and a configurable register with programmable clock, clock enable, clear and preset functions

The EPF10K20 device is a member of the high-density FLEX10K family. It comes in a 240-pin RQFP package. It has 1,152 logic elements and 6 embedded array blocks and a typical gate count of 20,000 gates. This paper discusses the EPM7128S device, which has been our primary implemented device.

Before using the EPM7128S device, locate the following parts (3):

- the EPM7128S which is a rectangular chip mounted to the board in a plastic socket. It is labeled “ALTERA MAX EPM7128SLC84-& AEH179731”.
- The EPM7128S Prototyping Headers which is a 2x11 array of prototyping headers.
- the JTAG_IN header, which is the 10-pin female plug on the ByteBlaster download cable, connects with the JTAG_IN 10-pin male header.
- the 2 octal dip-switches, the MAX_SW1 and MAX_SW2. They are below the PLCC package. They provide the logic level signals
- the DC_IN & Raw Power Input. It is located to the left and above of the PLCC package.
- The power LED which is located to the right and below of the JTAG.
- The TDI, TDO, DEVICE, and BOARD jumpers. They are located immediately above the PLCC package and below the JTAG plug.

Hooking up the UP1 Education Board to the PC

Setting the On-Board Jumpers

To program the EPM7128S device, the jumpers TDI, TDO, DEVICE, and BOARD should be set to C1 and C2 as shown in Figure 1.

Connecting the ByteBlaster Parallel Port Download Cable

The ByteBlaster Parallel Port Download Cable is provided by the manufacturer along with the UP1 Education Board. It is used to download data from the PC's parallel port to the circuit board. It has two connections:

- a 25-pin male header that connects to the PC parallel port
- a 10-pin female plug that connects to the circuit board.

Designing, compiling and simulating the program

In MAX+PLUS II 7.21 Student Edition, design, compile and simulate an error-free circuit to solve a given problem. For instructions on how to use the software for these tasks refer to the MAX+PLUS II 7.21 Student Edition Usage Guide located at the Wayne State Altera Web Site, http://ozric.eng.wayne.edu/~altera.

Programming the EPM7128S PLCC device

1. Open up the project. The name of the project must appear at the title bar of the window.

2. Click on Assign | Device. For Device Family, select the MAX7000S family. For Devices, select the EPM7128SLC84_7 (Figure 1).

3. Click on MAXII | Compiler | Start. The software will compile for the device that was previously selected. When done, it will state any errors or warning. There should be no errors.

4. Click on MAX+PLUS II | Programmer. The first time, the software requires that you perform the hardware setup. The Hardware Setup dialog box appears. For Hardware Type, select ByteBlaster. For Parallel Port, select the Port that the ByteBlaster download cable is connected to on your PC. Click on OK to close the Hardware Setup dialog box and save the changes.

5. Maximize the Programmer dialog box. At the right hand side, the file, device and checksum are listed. For example the file is the filename.pof, the device is the EPM7128SLC84-7, and the sum is 001dEE78.

6. Click on Program. MAX+PLUS II will examine, program and verify. While programming the device, the middle green LED on the board will be flickering indicating progress.

7. Programming of the hardware device is now complete.

Testing the programming of the EPM7128S device

You can now test the successful programming of the device with the designed circuit.

1. You need to identify the inputs and outputs of your design.
2. You now need to physically feed the inputs to the device and receive the outputs from the device.
   (a) To feed the inputs to the device, physically connect the dip switches to the PLCC package prototyping headers. You will need to identify which of the 84 connections of the 4 headers represent your inputs and will convey the digital data from the dip switches to the device correctly. To do so, consult the report of your circuit. The filename.rpt file displayed in the text editor shows the pin-out of the project indicating the headers representing the inputs and outputs.
   (b) To receive the output from the device, physically connect the output headers from the PLCC package to the LEDs. You can identify the output headers using the report of the circuit. You can now test the program.

VI. Conclusion

In this paper, we showed the implementation of a digital laboratory using Altera Development Package. We have created a laboratory manual which contains instructions on how to use the graphical editor, how to compile and simulate a project. The web site for this manual is http://ozric.eng.wayne.edu/~altera. In this paper, however, we showed the hardware implementation of our project using the UP1 Education Board.

The impact of our project is wide. Its impact on engineering technology education at WSU is realized through the addition of new laboratory designs using state-of-the-art CPLDs in all required digital design and computer architecture courses. Our students in Digital Design and Microcomputer Hardware Design courses have informed us that they have benefited from this laboratory enhancement. Its impact on K-12 education will be even deeper with the planned teacher training workshops on digital design technology.

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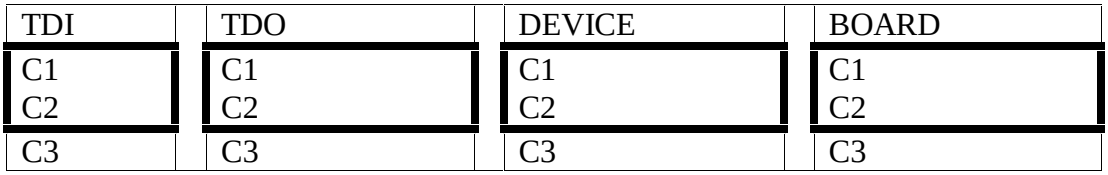

Figure 1: Setting the Device On-Board Jumpers