

Automated Measurement of MOS Capacitance and Determination of MOS Process Parameters in The MicroFabrication Laboratory

**Mustafa G. Guvench
University of Southern Maine**

Abstract

This paper describes, (1) how to inexpensively automate measurement of MOS diode C-V characteristics by employing standard test equipment available in a computer integrated electronics instructional laboratory, and (2) a technique that facilitates accurate extraction of MOS and structural parameters such as the threshold and flatband voltages, the gate oxide thickness, and the semiconductor doping concentration from the acquired data for the evaluation of an MOS device fabrication process in a microfabrication laboratory. Low cost, simplicity, and accuracy warrant adoption of both for instruction as well as research. The extraction technique is based on a nonlinear mapping of the C-V data which helps clearly demarcate the three modes of the MOS operation, accumulation, depletion, and inversion. It is also shown that the slope of the resulting curve yields an accurate measure of the semiconductor substrate doping. The technique and its accurate yielding of doping have been verified theoretically with MathCad simulations. The measurement setup and the extraction technique have been used to evaluate the MOS samples made in-house as part the microfabrication course taught at the University of Southern Maine.

1. Introduction

The Metal-Oxide-Semiconductor structure, universally referred as the “MOS”, beside forming the basis of the working of the MOS Field Effect Transistor (MOSFET) which is the backbone of our integrated circuits, lends itself as a diagnostic tool for determining the quality of the process used in the fabrication of an integrated circuit. Therefore, it constitutes an essential part of semiconductor wafer fabrication as well as semiconductor device physics and deserves emphasis as an instructional tool and fundamental background status in the microelectronics education, both undergraduate and graduate [3]. However, the equipment available for MOS capacitance testing is either too specialized and expensive, making it a “push-button” experience and unaffordable, or very crude and manual, making it too time consuming to use as an instructional tool in a class setting. Detailed discussions of the MOS physics, MOS capacitance theory and measurements can be found in the literature (Sze [5], Streetman [6] and Schroder [7]). Simply stated, the MOS structure, since it is a sandwich of conductor-insulator-semiconductor, constitutes a capacitor whose capacitance varies in response to the total voltage applied (please see Figure 1). This variation is due to the semiconductor which can be depleted of its majority

carriers to a certain depth by the repulsive electric field forces created by the voltage applied to the metal (gate) and effectively adding another insulating layer of variable thickness to the oxide above it. Therefore, the capacitance, starting from its maximum which is for fields attracting the majority carriers to the semiconductor's surface (the "accumulation" mode) decreases steadily as the field is reversed to cause "depletion" of them near the surface until the oppositely charged minority carriers are attracted in large numbers to the oxide interface to shield the depletion layer from further increases in the field. At that point (1) the depletion thickness stops increasing, and (2) its capacitance is compromised by a leakage resistance due to the traffic of the minority carriers from the bulk to/from the inversion layer. In a MOSFET structure the device starts conducting through the inversion layer, i.e. it turns on. In the accumulation and depletion modes the minority carriers due to their small number cannot affect the C-V characteristics. However after the onset of inversion and particularly at low frequencies when the depletion capacitance has a high impedance they can effectively short it with the leakage resistance they introduced in parallel and bring the measured capacitance back up to the oxide capacitance value. At high frequencies (1 MHz and above) this effect is minimal as well as the complications introduced by interface states between the semiconductor and the oxide [5]. Therefore, high frequency C-V measurements are preferred when the minority carriers and their interaction with interface states are not of interest.

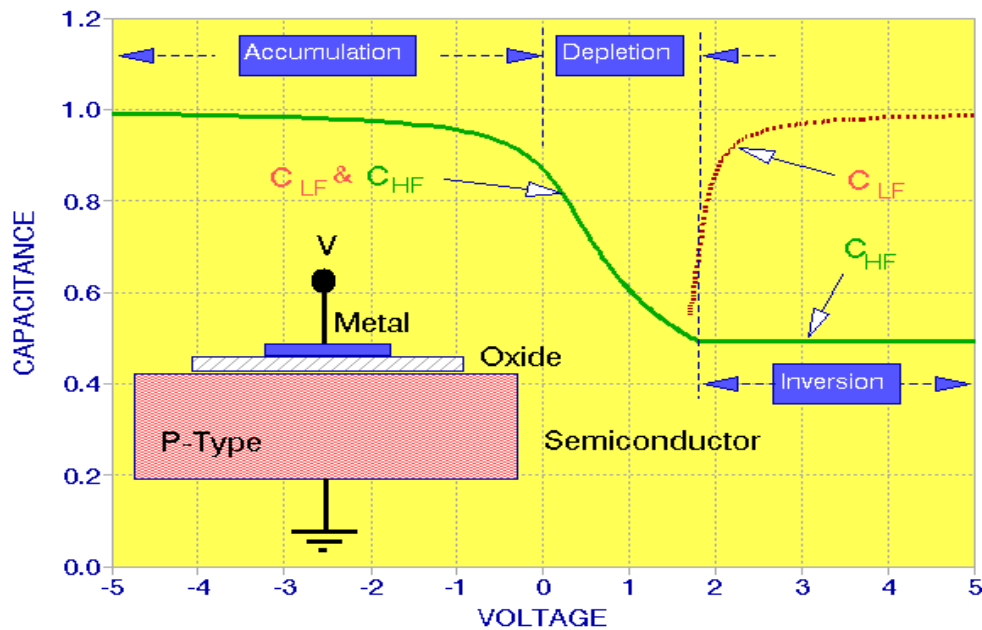


Figure 1. MOS Structure and C-V Characteristics

In this paper a C-V measurement set-up built by adding an inexpensive 1 MHz capacitance meter to the standard computer-integrated-electronics laboratory benchtop equipment is shown to be effectively used to evaluate the quality of the MOS structures processed in a MicroFabrication laboratory. The tools required are a standard computer-integrated-electronics^(1,2,3) laboratory bench set comprising of one each of GPIB interfaced digital multimeter, digital oscilloscope,

function generator, and a DC power supply. The GPIB interfaced instruments are controlled by a personal computer which serves for data acquisition and data processing as well as control. Such computer-integrated-electronics laboratory setups are replacing non-computer-interfaced equipment in electrical engineering laboratories. Guvench has shown that such laboratory equipment can be used to serve not only as electronic test bench but for in-situ tools for electronic design automation, design verification, device characterization, and SPICE model parameter extraction as an integral part of undergraduate electronics/ microelectronics/VLSI curriculum [1,2,3].

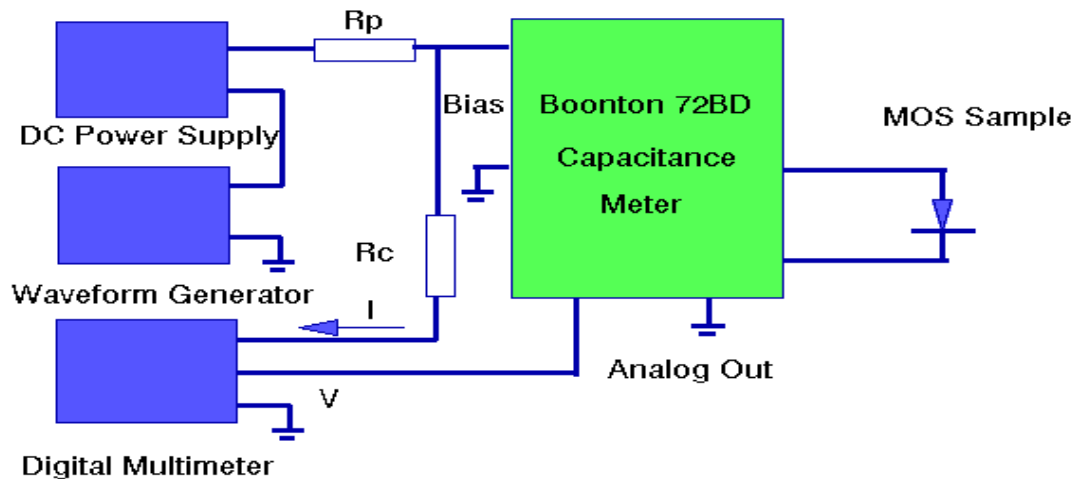


Figure 2. The C-V Measurements Setup

With the addition of a Boonton 72BD 1 MHz capacitance meter which comes with analog and digital outputs and with the appropriate software to interface the personal computer this setup is converted into an automated capacitance-voltage measurement system. The software, given the range of the voltage bias, sweeps the bias to cover the accumulation through the depletion into deep inversion and creates a data file in a suitable format which can be imported into any standard spreadsheet program for data processing and plotting. QuattroPro has been used to extract MOS oxide parameters such as the oxide thickness and capacitance, the MOS threshold and flat band voltages, the interface state charge, and interestingly, the semiconductor substrate's doping concentration. The same setup can also be used for Schottky and P-N junction capacitance measurements for doping, barrier-height, and built-in potential determination, or for determining bipolar and FET transistor SPICE model capacitances. In this paper we are concentrating on the use of such a setup as a tool for evaluating the quality of the MOS structures made in a MicroFabrication laboratory as an enhancement to a Silicon Device Fabrication course.

2. The Automated C-V Measurement Setup

The computer-integrated-electronics equipment set used consists of a 120 MHz 586 PC controlling via IEEE 488 bus a Tektronix AFG 5101 arbitrary waveform generator, a Tektronix DM 5120 digital multimeter, a Hewlett-Packard HP 54501 digital oscilloscope, and a Tektronix PS 250 dc power supply. This set is suitable for ac/dc current, ac/dc voltage and dc resistance measurements.

For MOS C-V measurements the sample needs to be applied a bias voltage which will be stepped from accumulation to inversion, and a small signal sinusoidal source (about 10 mV amplitude) for capacitance determination. Although, in principle, it is possible to use the equipment listed above to measure impedance, therefore a pure capacitance, the bandwidth of limitations of the multimeter and the resolution of the oscilloscope precludes such an attempt. A Boonton 72BD 1 MHz capacitance meter which has a capacitance range of 0 - 2000 pF was preferred. The Boonton 72BD is inexpensive and has an analog output and a bias input port separate from the sample connections for noninterference with parasitic capacitance from the bias connection. It also allows shielded connection to a sample box for low noise. The sample box contained a vacuum chuck with embedded heater and thermocouple facilitating also temperature cycling for oxide ion drift experiments. Figure 2 gives a schematic representation of the setup.

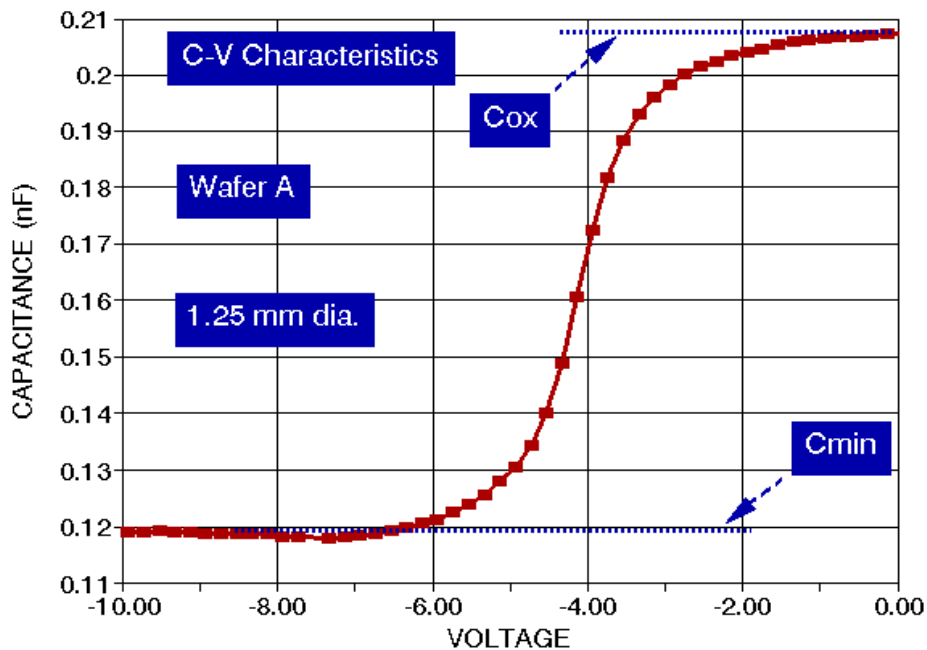


Figure 3. Measured MOS C-V Characteristics

A home developed data acquisition software named “CIE-IV3.EXE”, originally written in Quick Basic for automated measurement of transistor I-V characteristics was modified to sweep the waveform generator as a stepped dc bias source and measure the C-V characteristics by relying on the Boonton capacitance meter to do the conversion from capacitance to dc voltage. The setup has only one meter. Guvench’s [2,3] technique of switching the multimeter between the voltmeter and the ammeter modes was employed to save from the cost of adding a second multimeter to the setup. The digital multimeter, under the control of the CIE-IV3 software to be in its “DC Volts” mode first measures the bias voltage applied to the sample through its voltage input terminal. It is then switched to the “DC Amps” mode to measure the dc current passing through its current input terminal. The sample’s capacitance is indirectly measured through this current which is generated by a calibrated resistor connected to the analog output of the capacitance meter. The “CIE-IV3” program generates “comma delimited” ASCII files of the capacitance against the bias voltage, which can be imported into QuattroPro or Excel for graphing and processing. Figure 3 displays the C-V results obtained and graphed with QuattroPro for a sample measured in this way. The dc power supply shown connected in series with the stepped waveform generator is for the purpose of supplementing the limited range (± 9.8 V) of the waveform generator. Typically a 100 point data set measurement takes about 3 minutes, i.e., the sweep is slow enough to keep the MOS capacitance in quasistatic equilibrium in inversion to avoid undershooting into deep depletion.

3. Models for MOS Capacitance Characteristics

For an MOS structure built on a uniformly doped semiconductor the Poisson equation [5] can be solved exactly to get the electric field, E_s and the total charge the semiconductor has stored in its space charge (or depletion) layer, Q_s as a function of the electrostatic potential ψ_s its surface has reached under the influence of the gate field applied. The resulting equations are given below.

$$E_s(\psi_s) := \frac{\sqrt{2 \cdot k \cdot T}}{q \cdot L_D} \cdot \frac{\psi_s}{|\psi_s|} \cdot F(\psi_s)$$

$$Q_s(\psi_s) := \epsilon_{Si} \cdot E_s(\psi_s)$$

where $\beta = q / kT$ is the inverse thermal voltage, ϵ_{Si} is the dielectric permittivity of the semiconductor and Debye length given by

$$L_D := \sqrt{\frac{\epsilon_{Si}}{q \cdot p_{po} \cdot \beta}}$$

is the extrinsic Debye length. The semiconductor is assumed to be p-type with a majority carrier concentration of p_{po} and a minority concentration of n_{po} . $F(\psi_s)$ is a function defined as ,

$$F(\psi_s) := \sqrt{\left(e^{-\beta \cdot \psi_s} + \beta \cdot \psi_s - 1 \right) + \left(\frac{n_{po}}{p_{po}} \right) \cdot \left(e^{\beta \cdot \psi_s} - \beta \cdot \psi_s - 1 \right)}$$

The total voltage appearing across the MOS structure is the summation of the voltage drop in the oxide and the voltage drop in the semiconductor (i.e. its surface potential).

$$V_{MOS}(\psi_s) := \psi_s + \frac{Q_s(\psi_s)}{C_{ox}}$$

Note that the derivative of the charge with respect to the surface potential gives the effective capacitance of the semiconductor's space charge layer. It can be shown that this capacitance is given by

$$C_{DLF}(\psi_s) := \left(\frac{\epsilon_{Si}}{\sqrt{2} L_D} \right) \cdot \left[\frac{\left(1 - e^{-\beta \cdot \psi_s} \right) + \frac{n_{po}}{p_{po}} \cdot \left(e^{\beta \cdot \psi_s} - 1 \right)}{F(\psi_s)} \right] \cdot \left(\frac{\psi_s}{|\psi_s|} \right)$$

which has to be connected in series with the oxide layer's capacitance $C_{ox} = \epsilon_{Si} / t_{ox}$, resulting in

$$C_{LF}(\psi_s) := \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_{DLF}(\psi_s)}}$$

Note that in all of the above minority carriers are included via the terms involving n_{po} in the equations. Therefore, the resulting capacitances will correspond to the low frequency (LF) measurements. If the high frequency C_{HF} -V curves are needed the equations written above can be used by eliminating n_{po} multiplied terms which stand for the minority carriers. However, such an elimination also takes out the screening effect of the inversion layer on the space charge, resulting in a representation of a case named "deep depletion". A simple solution is to employ the majority-carrier-only equations until the surface potential reaches a value corresponding to the onset of heavy inversion. This condition is taken as $\psi_s = 2 \cdot \phi_{FP}$ where

$$\phi_{FP} := \frac{k \cdot T}{q} \cdot \ln \left(\frac{N_A}{n_i} \right)$$

Beyond that point the capacitance is taken to have reached a flat minimum. Although the equations written above do not lead to a closed form for CLF and CHF vs terminal voltage, their curves can be plotted by stepping the common variable in them, i.e., ψ_s . MathCad has been found to be a powerful and convenient tool for this purpose. As a matter of fact the curves given in Figure 1 are the results of such calculations with the exception that the capacitances plotted are normalized with respect to the oxide capacitance.

It is noted that neither the experimental C-V curve of Figure 3 nor the theoretical curves of Figure 1 display sharp changes that can identify the transition points between accumulation and depletion (named the flatband voltage, V_{FB}) nor between depletion and inversion (named the threshold voltage, V_T). Therefore, MOS C-V curves cannot deliver precise values for the flatband voltage, V_{FB} nor the threshold voltage, V_T .

A nonlinear mapping/transformation of the C-V relationship was sought that would render a sharp transition between the modes of MOS operation. Figure 4 shows the result of plotting $1/C^2$ vs MOS bias voltage instead of linear capacitance versus voltage. In these plots “ICS” is used to mean “Inverse-Capacitance-Squared”. Both high frequency and low frequency capacitances are included for comparison, and an approximate capacitance calculated using “depletion approximation” as well. All of the resulting curves strikingly show straight line behaviour in the depletion region. It is also observed that the intersection of this straight line with the asymptotes of minimum and maximum capacitance yield exactly zero for MOS bias at the flatband transition and exactly $\psi_s = 2\phi_{FP}$ at the inversion threshold point. This behaviour was consistently displayed by all samples whose doping concentrations were varied between $10^{14}/\text{cm}^3$ and $10^{16}/\text{cm}^3$ implying a universality. ..

The “depletion approximation” capacitance calculations are done by assuming that (1) the space charge in the semiconductor is solely due to majority carriers, and (2) the space charge edge is abrupt at a depth of x_d . These conditions imply the total space charge to be $q \cdot N_A \cdot x_d$, and the MOS voltage drop and capacitance to be

$$V(x_d) := \frac{q \cdot N_A \cdot x_d}{C_{ox}} + \frac{q \cdot N_A \cdot x_d^2}{2 \cdot \epsilon_{Si}}$$

$$C(x_d) := \frac{1}{\frac{1}{C_{ox}} + \frac{x_d}{\epsilon_{Si}}}$$

Note that IC stands for inverse of capacitance and ICS stands for inverse-capacitance-squared. Then,

$$d(ICS)/dV = 2 \cdot (IC) \cdot (d(IC)/dV) = 2 \cdot IC \cdot (dx_d/dV) / \epsilon_{Si}$$

From above, $dV/dx_d = q \cdot N_A \cdot IC$, and therefore,

$$d(ICS)/dV = 2 / (q \cdot N_A \cdot \epsilon_{Si})$$

This last expression shows that the slope of the ICS versus bias voltage curve in the depletion region is a constant as observed and it conveniently measures the doping concentration of the semiconductor.

4. The Extraction Procedure

The section above has shown that,

- (1) Square of the inverse-capacitance-of an MOS structure is expected to be vary linearly with the applied bias voltage in the depletion region;
- (2) Its slope yields the doping concentration;
- (3) Its intersection point with the maximum capacitance asymptote yields the flatband voltage, V_{FB} ; and
- (4) Its intersection point with the minimum capacitance asymptote yields the onset of heavy inversion or the threshold voltage, V_T .

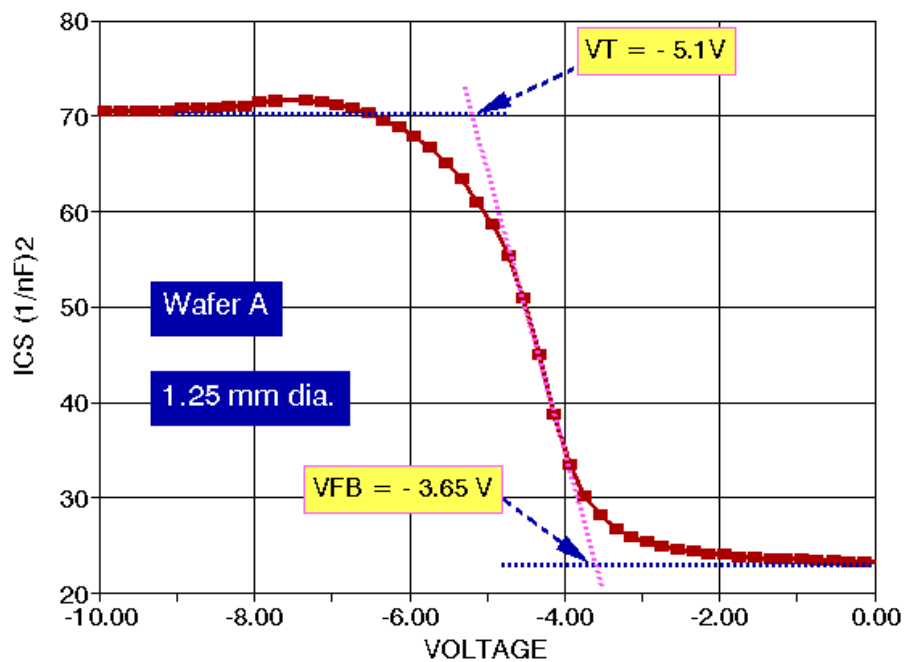


Figure 5. Inverse-Capacitance-Squared Curve

The conclusions drawn above were applied to evaluate the MOS capacitor sample whose high frequency C-V curve is shown in Figure 3. Note that the capacitance minimum of the experimental C-V curve is on the left, implying that the MOS sample was actually built on an n-type rather than a p-type semiconductor. The simplicity of the mathematical manipulation involved allowed a spreadsheet program such as the QuattroPro to be employed without necessitating custom-made programming to be developed in a high level language.

Figure 5 depicts the ICS values calculated and plotted as a function of the bias voltage. Also included are the asymptotically drawn three straight line segments. The segment in the middle represents the depletion region where the ICS curve is expected to behave like a straight line, and it does. In this range the slope is also at its maximum. The other two are the asymptotes

corresponding to the minimum and the maximum capacitance. From the intersection points of the straight lines the flatband voltage is determined to be - 3.65 volts, the threshold voltage to be - 5.1 volts. The maximum capacitance value of 207 pF, with the area calculated from the 1.25 mm diameter of 0.01227 cm^2 yields the oxide thickness to be 2056 Angstroms. Note that the ICS values plotted include the area of the capacitor. Therefore, in the slope calculations square of the area multiplies the slope read from Figure 5. The slope value calculated (4.83×10^{15}) predicts the doping of the semiconductor to be $2.5 \times 10^{15} / \text{cm}^3$.

The flatband voltage of an MOS capacitor is affected by the metal-semiconductor work function difference, ϕ_{MS} and the charges residing in the oxide and at the semiconductor-oxide interface. The contribution of the latter depends on their distribution relative to the interface as well as their density. The distribution cannot be obtained from the flatband voltage. However, by making the assumption that these charges are concentrated at the oxide-semiconductor interface one can write,

$$V_{\text{FB}} = \phi_{\text{MS}} - Q_{\text{ss}} / C_{\text{ox}}$$

Using $\phi_{\text{MS}} = 0.28$ volt from Streetman[6] the equivalent interface charge density (Q_{ss} / q) is determined to be 3.5×10^{11} charges / cm^2 for this sample.

5. Discussions and Conclusions

The samples were prepared from 3-inch diameter N-type (111) cut Silicon wafers with nominal resistivity range of 1 - 8 ohm-cm. This corresponds to an approximate range of $(0.5 - 4) \cdot 10^{15} / \text{cm}^3$ doping concentration. The wafer "A" had measured a doping level of $2 \cdot 10^{15} / \text{cm}^3$ with a four point resistivity probe prior to the processing which is consistent with the doping value extracted above. Wafers were dry oxidized at 1050 degrees Celcius at varying times to yield oxide thicknesses from 1000 to 4000 Angstroms. Aluminum dots of 1.25 mm diameter were formed via vacuum vapor deposition in a turbomolecular pumped Denton 602 vacuum system. Each 3-inch diameter silicon wafer made a total of 264 of the 1.25 mm diameter Aluminum gate circular MOS diodes, large enough in number for use in a class setting as an enrichment project for a microfabrication course taught by the author at the University of Southern Maine.

The measurement setup and the MOS procedures outlined in this paper were used by the students to characterize the distribution of the doping density, oxide thickness, flatband and threshold voltages and the interface equivalent oxide charge on these wafers with success.

The C-V measurement results obtained from them turned out to be consistent with the expected values of oxide thickness, doping and fixed oxide charge showing that the technique presented and the procedure outlined in this paper were reliable and useful in addition to being simple and inexpensive, therefore, suitable for instructional use as well as research.

.....

REFERENCES

- [1] Guvench, M.G., "USM Computer-Integrated- Electronics Laboratory," Proc. of A.S.E.E., Vol.1, pp.337-340, 1992.
- [2] Guvench, M.G., "Automated Measurement of Semi- conductor Device Characteristics For Computer Assisted Electronic Design," Proc. of A.S.E.E. Conf., Vol.1, pp.671-675, 1993.
- [3] Johnson, D.A. and Thompson, M.G., "Undergraduate Semiconductor Characterization", Proc. of A.S.E.E., Vol.1, pp.565-569, 1994.
- [4] Guvench, M.G., "SPICE Parameter Extraction From Automated Measurement of JFET and MOSFET Characteristics In The Computer-Integrated-Electronics Laboratory", Proc. of A.S.E.E., Vol.1, pp.879-884, 1994.
- [5] Sze, S.M., *Physics of Semiconductor Devices*, 2nd. ed., John Wiley, 1981.
- [6] Streetman, B.G., *Solid State Electronic Devices*, 3rd. ed., Prentice Hall, 1990.
- [7] Schroder, D.K., *Semiconductor Material and Device Characterization*, John Wiley, 1990.
- [8] "MathCad" is a product of MathSoft, Inc., Cambridge, Massachusetts.

MUSTAFA G. GUVENCH

Mustafa G. Guvench was born in Adana, Turkey in 1946. He received his B.S. and M.S. degrees in Electrical Engineering from M.E.T.U., Ankara in 1968 and 1970, respectively. He did further graduate work at Case Western Reserve University, Cleveland, Ohio between 1970 and 1975 and received M.S. and Ph.D. degrees in Electrical Engineering and Applied Physics. He is currently a full professor of Electrical Engineering at the University of Southern Maine. Prior to joining U.S.M. he served on the faculty of M.E.T.U., Ankara and Gaziantep campuses, Turkey and the University of Pittsburgh. His research interests include microelectronics technology and its application in sensor development, finite element and analytical modeling of semiconductor devices and sensors, and electronic instrumentation and measurement.

Acknowledgements

This work would not have been initiated and made possible without grants from the National Science Foundation (Grant No. USE-905 1602) and the Masterton Foundation, both of which provided the funds to establish the "Computer-Integrated-Electronics Laboratory" at the University of Southern Maine.