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Circuit-Level Microelectronics Reliability Project to Foster Interdisciplinary Engineering Learning

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Abstract

The Microelectronics Reliability course has been offered in the Division of Engineering Programs at SUNY New Paltz as a professional elective since Spring 2020. As one of the pedagogical goals of this one-semester course is to highlight and promote the interdisciplinary nature of semiconductors engineering, students are encouraged to collaborate and contribute their technical knowledge in the realms of electrical and mechanical engineering to study the reliability of computer chips. In the past, this course introduced the degradation mechanism associated with each circuit component separately, including hot-carrier injection in transistors and electromigration in metal interconnects. Individual projects were assigned to model and project the end-of-life wear-out from a specified degradation mechanism. The prior course did not engage direct collaboration between the electrical and mechanical engineering students. Since interdisciplinary collaboration and apt technical communication are necessities in the semiconductor industry, an effective delivery of this course engenders the development of a team-based project in which students in different disciplines can exercise their respective academic knowledge bases to jointly make reliability assessments. We propose a final team project which studies the overall circuit-level reliability, with each group comprising a mix of two to three mechanical, electrical and computer engineering students. Employing a basic BiCMOS voltage follower, groups are required to conduct circuit-level reliability assessments holistically, tasking students with quantifying the interaction among devices under operation, estimating the degradation of individual components, and proposing strategies to mitigate potential reliability risks. For the team project, electrical and computer engineering students will be charged with evaluating an assigned circuit on a schematic-level and simulating the circuit operation, and mechanical engineering students will undertake thermal and mechanical analyses to account for localized Joule heating and its implication on the electrical and mechanical integrity of the circuit. Collaboratively across disciplines, the condition of each circuit element under operation can be ascertained. This paper will introduce the design considerations and outline of the team project, as well as demonstrate the feasibility of the reliability assessment using the voltage follower circuit. Mean-time-to-failure for each relevant failure mechanism will be assessed as well as design shortcomings and improvements in reliability.

Introduction

As the complexity of technological innovation and advancement increases, the need for engineering scientists to pursue interdisciplinary industry-oriented research is greater than ever; this has been especially true for the semiconductor industry in recent years. In [1], Mody makes clear that the pursuit of microstructure fabrication involves a wide array of disciplines, from condensed matter physics, materials science, and electrochemistry to niche subfields such as electron microscopy. The integrative nature of microelectronics has been emphasized since the 1970s, with governmental funding for interdisciplinary research centers being especially notable. Prevailing the engineering science landscape, it is undeniable that developing advanced computer chips requires cross-discipline collaboration, technical support and communication. As we have previously shown in [2], interdisciplinarity can be practiced in the classroom, giving students a head start on professional development and career choice.

The Division of Engineering Programs at the State University of New York (SUNY) at New Paltz is home to an eclectic cast of undergraduate engineering programs, including computer engineering (CE), electrical engineering (EE) and mechanical engineering (ME); there is also a graduate-level master's EE program. Since the Spring of 2020, for three semesters, Microelectronics Reliability has been offered to the student body as a 400/500-level one-semester professional elective – many students who have taken this course have found their first job post-graduation in the semiconductor industry as process and equipment engineers. While the design of this course is discussed in [2], so too are the cross-disciplinary motivations underlying the pedagogy. In summary, the course has been successful in its implementation and emphasis of interdisciplinary learning and individual projects. This work expounds on our previous report, positing that this interdisciplinary endeavor should start in the classroom, commencing with a collaborative team project among EE, CE and ME students. We present a final course project for the class entitled Microelectronics Reliability, which will allow students of different academic disciplines to cooperatively assess the reliability of a voltage follower circuit, identify the weak points with reliability exposure, and report the results with a proposed risk mitigation strategy. Several skills across engineering disciplines will be highlighted, ranging from circuit and waveform simulation, stress/strain analysis, to heat transfer modeling.

Course Overview

As mentioned in [2], Microelectronics Reliability is a course devised to provide a platform to establish interdisciplinarity and communication between EE, CE and ME disciplines, as well as the opportunity for students to apply technical skills to problem solving in unfamiliar areas. Students in past semesters offered positive feedback in the context of cross-discipline exposure. Also, primary learning objectives of this course include applying fundamental science and engineering principles to solve practical and multidisciplinary problems to motivate students [3], as well as collaborating and communicating proficiently across different engineering disciplines [4]. Whereas our previous work outlines the structure and the intent of the course, it is worthwhile to provide the scope of its instructional design. It is noteworthy that the final team project discussed in this paper was proposed in the original course design as a critical component to exercise interdisciplinary teamwork – it has not been implemented due to the COVID-19 pandemic and limitations of software resources necessary for integrated circuit (IC) layout and simulation.

Before explicating the design of the final team project, the design of individual projects shown in Figure 1 merits discussion as learning projects are an important facet of interdisciplinary engineering education [5]. Two individual projects were implemented in the course, one involving analysis and research of a front-end-of-line (FEOL) transistor degradation mechanism termed hot-carrier injection (HCI), and one involving the modeling of a back-end-of-line (BEOL) metal interconnect wear-out mechanism called electromigration (EM). In each assignment, raw data was provided to students for analysis and establishment of an empirical model, in which equation parameters were extracted and projected product lifetime was determined. Though, in accordance with the planned learning outcomes, the individual projects proved to be effective in acquiring the technical knowledge outside the majored disciplines [2], they did not encourage partnership across disciplines. Also, students were only asked to analyze the reliability of a device from the experimental data collected under specific conditions; such individual projects had limited scope and did not provide enough practical relevance to the circuit operation. From an interdisciplinary viewpoint, HCI involved not only electrical biasing and transistor operation, but also local temperature of the transistor as well as interface

mechanics (between Si and SiO_2). On the other hand, EM modeling necessitated basic circuit design, Kelvin testing, thermal and mechanical stress analysis, and knowledge of diffusion mechanics (through crystalline metals). Therefore, the final team project proposed in this paper is aimed to provide an efficient platform for interdisciplinary collaboration in assessing and identifying the reliability of a simple circuit holistically, involving knowledge and skills in electrical, mechanical and materials engineering.

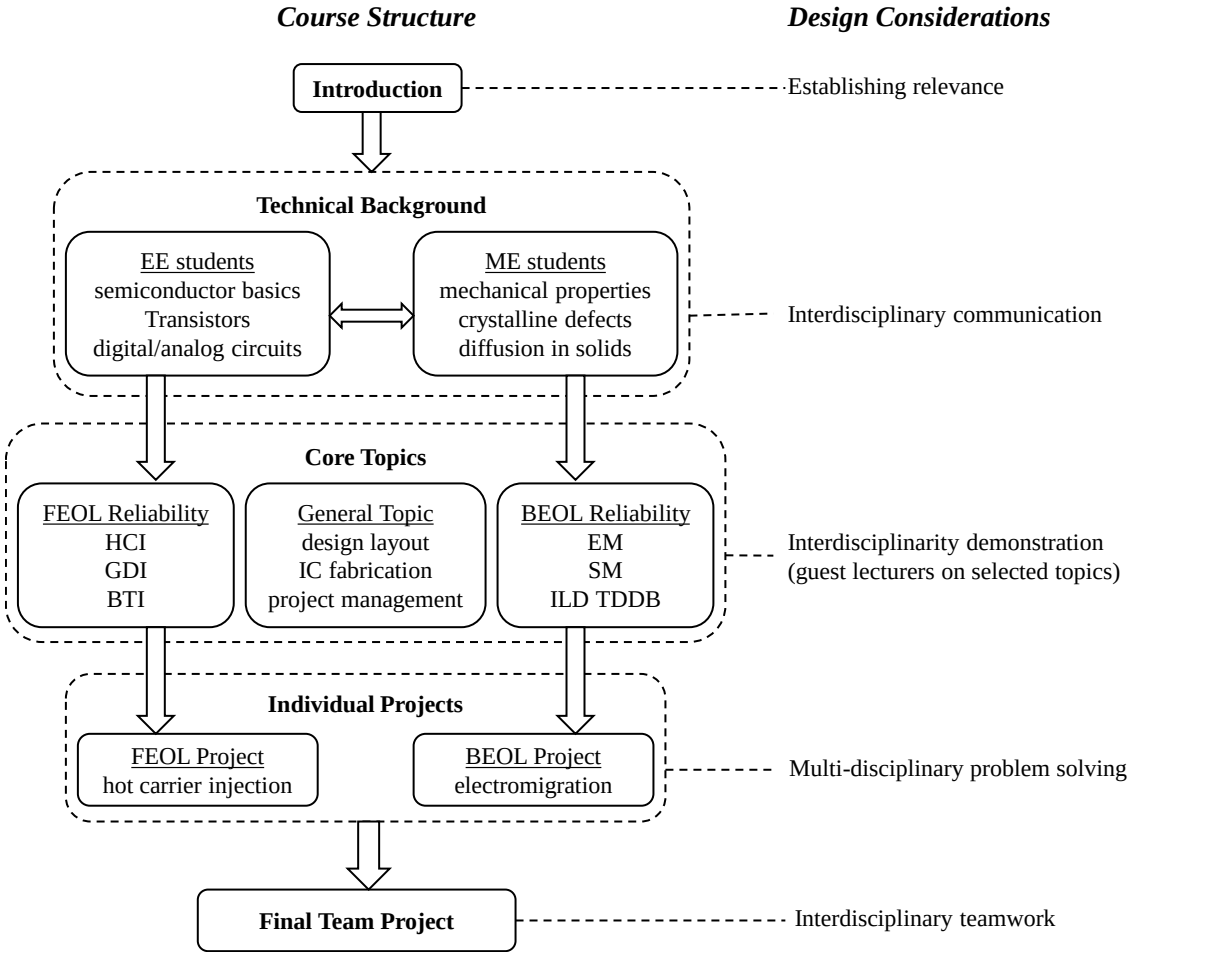

Figure 1. Outline of course structure with corresponding design considerations (adapted from [2] with permission).

Overview of Proposed Team Project

In this paper, we propose a final team project surrounding the reliability assessment of an integrated NPN common-collector amplifier circuit (or the so-called emitter follower, as illustrated in Figure 2); this circuit is prevalent in many IC applications [6]. The reasons for choosing this circuit are its simplicity and its inclusion of key circuit elements that are included in conventional reliability studies: bipolar and MOSFET transistors, resistors, as well as a capacitor. Furthermore, this circuit is a good candidate for a reliability study because of excessive power dissipation expected in the NPN bipolar junction transistor (BJT), unity voltage gain without stability concerns, and wide bandwidth.

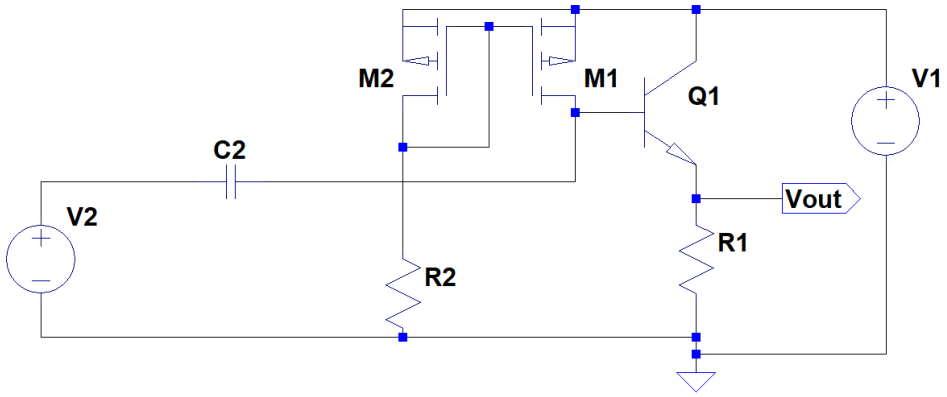

Figure 2. Emitter follower with biasing current mirror as the assigned circuit for reliability assessment for the final team project.

The proposed emitter follower circuit will follow the conventional configuration, where a PMOS current mirror will be used for biasing at base of the bipolar transistor. This relatively simple and functional circuit has two voltage sources V_1 (DC) and V_2 (sinusoidal AC), a decoupling capacitor C_2 on the input side, a load resistor R_1, a biasing resistor R_2, an NPN BJT Q_1, and two PMOS transistors M_1 and M_2 for the current mirror. Additionally, the output voltage V_{out} is at the emitter of Q_1 as shown in Figure 2. Teams of three students (with at least one ME and one EE/CE) will be provided with relevant reliability guidelines and limitations, required operating conditions (such as 5V as the technology voltage for V_1 in this example), and lifetime expectations. The physical design and dimensions of each circuit component is subject to engineering judgment by each group, based on performance and reliability considerations. For example, a use target for the maximum current density j_{use} of the metal interconnects will be provided as 10 mA/um^2 at 100 °C. This value needs to be adjusted according to specific operating conditions such as the local temperature of the interconnect under investigation, taking into account the Joule heating from adjacent power-dissipating elements. Through this team project, students are expected to acquire practical skills in incorporating reliability concepts in this circuit design endeavor collaboratively.

Each team needs to evaluate the corresponding degradation mechanism of critical circuit components, such as HCI of transistors and EM of interconnects, in order to address the overall circuit reliability. Two sets of information are necessary to achieve this. First, the electrical signal waveforms in each circuit component during circuit operation will provide detailed voltage bias and current profiles for degradation model calculations. Second, the physical dimensions and properties of each circuit element allow estimates of local temperature distribution and the resulting thermal stress under nominal operating conditions. The overarching intent of this project is for students to leverage individual strengths and exercise apt technical communication, with EE/CE students performing circuit simulation and ME students undertaking thermal and mechanical analyses. To illustrate the collaboration between different academic disciplines, Figure 3 shows a flow diagram that outlines the conceptual framework of the proposed interdisciplinary team project.

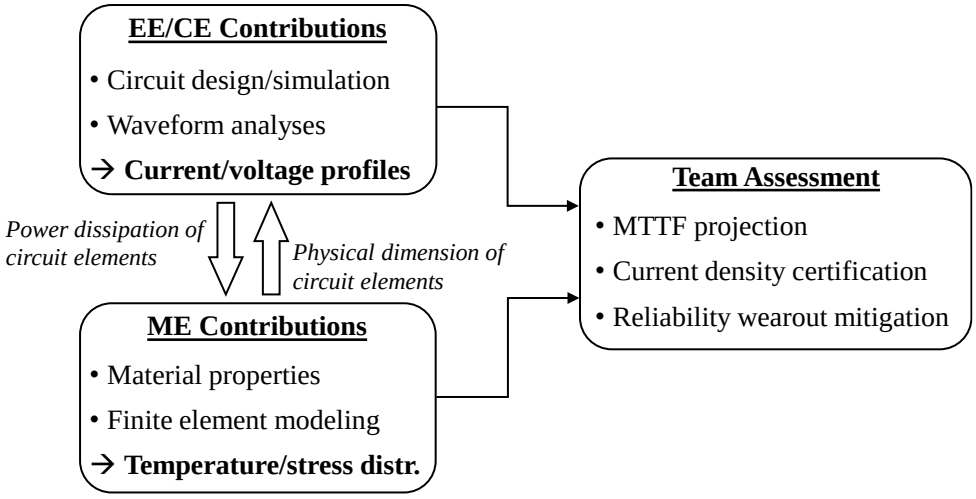

Figure 3. Conceptual framework of the proposed final team project with expectations and flow of information.

Expected Tasks from Electrical & Computer Engineering

By design, EE/CE students will possess the prerequisite knowledge to conduct circuit simulations and understand the operation of the circuit. Essentially, it is called an emitter-follower circuit because the output voltage V_{out} of the circuit "follows" the sinusoidal input V_2, while V_1 is strictly for DC biasing (and activates Q_1, M_1 and M_2). The ultimate idea of this buffer circuit, the emitter follower, is that it has a large input impedance and a small output impedance. The EE/CE students will recognize the advantages of this circuit, that it provides power and current gain, and a heavy resistive load will not drop the output. While students may not have the academic wherewithal or tools to perform layout-level electrical simulations of this circuit, they are expected to conduct a schematic-level simulation and to break up the circuit into simpler constituent parts to determine electrical characteristics that are pertinent to the reliability studies, as shown in Figure 4.

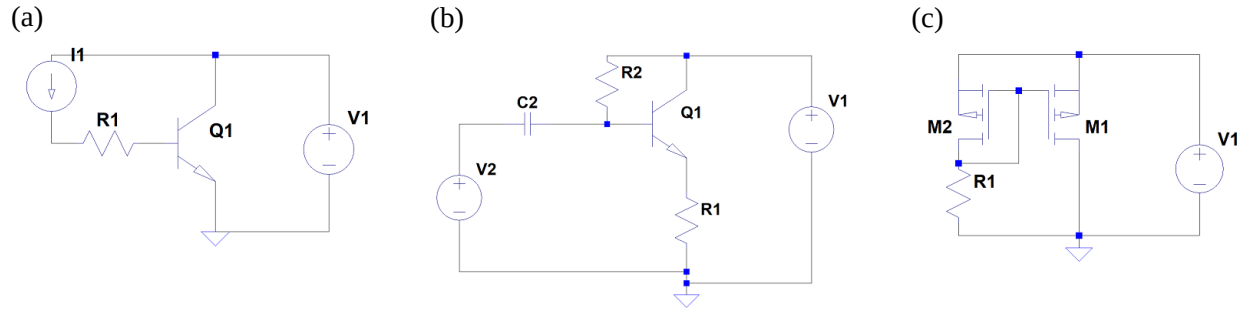

Figure 4. Circuit constituents for (a) BJT I-V characteristics and DC operating point determination, (b) BJT gain characterization, and (c) current mirror design.

A breakdown of the preliminary analysis should be undertaken by EE/CE students to determine the I-V and gain characteristics of the NPN BJT, shown in Figures 4(a) and 4(b), respectively, and define the aspect ratio of the PMOS transistors in the current mirror shown in Figure 4(c). Students will be provided with starting design parameters of this circuit, including the resistance and capacitance values of relevant elements for achieving the specific output V_{out}.

Recommendations for transistor models will also be provided (Gummel-Poon format for BJT and level 2 and above BSIM models for the PMOS transistors) [7]. EE/CE students are expected to demonstrate operation of the circuit and communicate to non-EE students its functionality and limitations.

After the preliminary analysis with the circuit constituents, EE/CE students will complete the design and simulation of the entire emitter follower circuit shown in Figure 2. They are expected to estimate the operating conditions for all circuit elements, such as the voltage and current profiles of each circuit element. For example, Figure 5(a) shows the simulation results of the emitter follower circuit that EE/CE students are expected to arrive at in terms of voltage, confirming the output V_{out} (in blue) is a sinusoid with a DC offset at the specified value. The V_{out} sinusoid should not be distorted or clipped, and it should be delivered with the same frequency as the input V_2 (in green). Figure 5(b) shows the simulated current waveforms at the base (in green), collector (in blue), and emitter (in red) of the BJT. In conjunction with the voltage waveform in Figure 5(a), the power dissipation of the BJT can be properly determined. Also, the current densities of the interconnects contacting the BJT can be obtained from the current waveforms, provided that the physical dimensions of the interconnects are available. These values contribute to the first set of information described in the previous section necessary for subsequent reliability assessment.

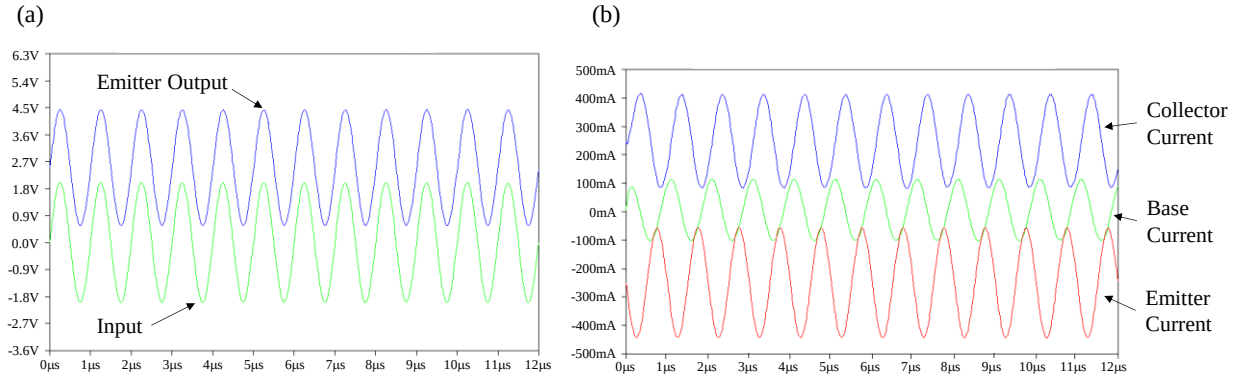

Figure 5. (a) Voltage waveform of the input and output of the emitter follower circuit, and (b) current waveform of the emitter, base, and collector of the BJT.

Expected Tasks from Mechanical Engineering

ME students will be expected to translate the emitter follower circuit into physical layout according to the provided list of process assumptions that include the relevant material properties (such as sheet resistance and thermal conductivity) and physical dimensions (such as layer thickness and doping depth). For example, Table 1 lists the specified sheet resistance and thickness of a few materials used in fabricating the circuit, from which ME students will be able to determine the physical dimensions (i.e., width and length) of each resistor and interconnect in the follower circuit according to the circuit design [8].

Table 1. Typical sheet resistances of different materials are provided to aid in resistor selection.

	Sheet Resistance (Ω/square)	Thickness (μm)
First-level metal wiring	0.10	0.5
P+ polysilicon resistor (unsalicided)	350	0.5
P+ polysilicon resistor (salicided)	8.0	0.5

With the physical model established for each circuit component and its contacting interconnects, along with the power dissipation determined by the EE/CE students described previously, finite element analysis (FEA, a required course for ME students at SUNY New Paltz) can be conducted to determine the self-heating and the resulting temperature distribution around each circuit component, particularly for the critical ones with expected high power dissipation such as the BJT and resistors, and the temperature of the contacting interconnects. Note that while the self-heating analysis and simulation of the BJT could be considered too complex for the scope of this team project, involving detailed knowledge of doping profiles and the corresponding current flow [9,10], ME students will thus be advised to either properly simplify the BJT physical model or choose the resistors for the FEA modeling.

Using the resistor R_1 as an example (see Figure 1), its physical model comprises the resistor layer of choice (e.g., salicided P+ polysilicon resistor in Table 1) and the interconnect structure contacting each end of the resistor for wiring. With the dimensions of the resistor layer and interconnect configuration defined according to the circuit design specifications and reliability guidelines, as illustrated in Figure 6(a), the 3-dimensional physical model can be constructed and imported to the FEA tool, as shown in Figure 6(b) [11].

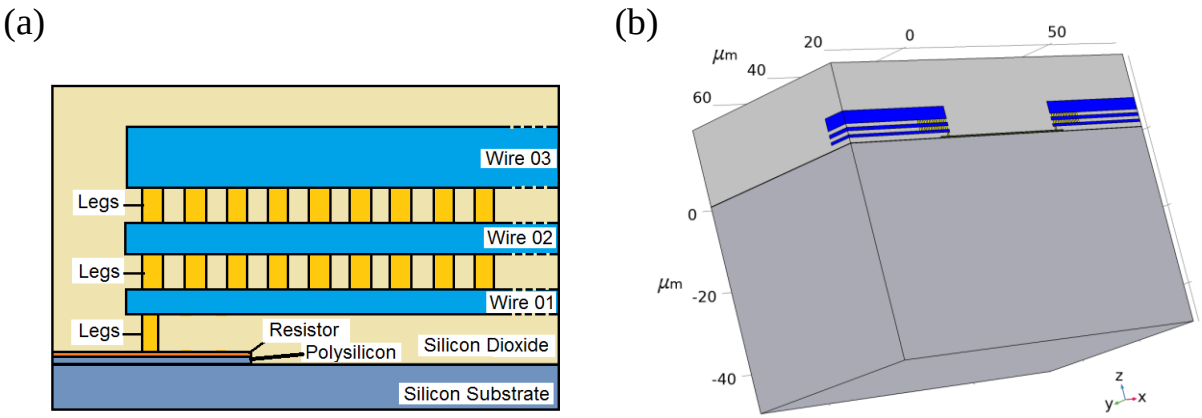

Figure 6. (a) Cross-sectional view of a resistor structure, with only half shown due to symmetry, and (b) the 3D physical construction used for FEA modeling (adapted from [11] with permission).

To conduct FEA thermal simulations, ME students will input the power dissipation of each circuit component to the model and apply adequate boundary conditions with sound engineering judgment. As an example, Figure 7 shows the resulting temperature distribution over the aforementioned resistor in false color [11], revealing the excessive Joule heating from power

dissipation in the resistor layer. Conditions of the neighboring materials can also be extracted, including the temperature of the contacting interconnects and the surrounding dielectric material. Together with the physical dimensions and material properties of the circuit components, this data contributes to the second set of information for the overall reliability assessment of the circuit.

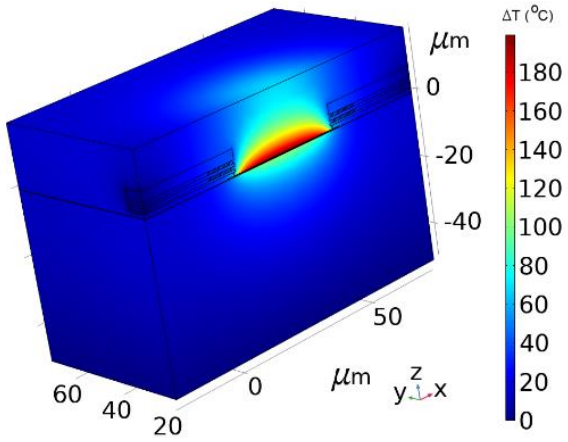

Figure 7. Temperature distribution of the modeled resistor structure under operating conditions (adapted from [11] with permission).

Overall Reliability Assessment and Project Deliverables

With the two sets of information obtained collaboratively, including the voltage bias, current density, and local temperature distribution for each circuit component and interconnect under operation condition, each team is expected to estimate all the relevant degradation mechanisms to assess the reliability risk of the circuit. Though in principle every component in the circuit should be addressed, judgement should be exercised to identify the most vulnerable areas of the circuit for detailed analysis. For example, one notable reliability concern of this circuit is the electromigration of the metal lines connecting the resistors with high power dissipation and Joule heating. Teams should be able to leverage their knowledge of this degradation mechanism in the context of the individual project on this topic. Based on the current density from the waveform analysis and the interconnect temperature from the FEA modeling, the expected lifetime of the interconnect and thus its reliability risk can be predicted through Black's equation, a widely accepted model for electromigration kinetics [12]. Additionally, it is also possible for ME students to consider and simulate the resulting thermal mechanical stress in the circuit due to device heating for potential implication on thermal fatigue failure. If there are outstanding reliability concerns, team will be expected to posit abatement strategies to mitigate reliability concerns as part of the project deliverables. For example, increasing line width, reducing power and selecting different materials are all viable strategies to bolster reliability – the circuit's operational performance should be unaffected by mitigation strategies.

Conclusions

To further develop the Microelectronics Reliability course as a platform to foster interdisciplinary engineering learning, a final team project is proposed for students to collaborate with technical expertise in different disciplines. Employing a basic BiCMOS voltage follower circuit, members in the multi-disciplinary team (comprising EE/CE and ME students) bring their

respective knowledge and skills to contribute equally to the project. EE/CE students are expected to exercise skills in circuit design and analysis to provide the team with electrical waveforms and power dissipation in each circuit components, while ME students are expected to conduct thermal analysis and material specification to provide distributions of local temperature and current densities within the circuit. All students will have the freedom to explore concepts in semiconductors and microelectronics and work together to make engineering judgements. Collaboratively, each team is expected to assess and identify reliability risks in the circuit and recommend mitigation strategies in a holistic approach.

Acknowledgement

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