AC 2007-949: CLOSING THE HARDWARE DESIGN LOOP WITH MULTISIM: A CASE STUDY

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Closing the Hardware Design Loop with Multisim®: A Case Study

Abstract

Most electronics courses taught these days are planned around what is called a lecture-and-lab environment. This environment traditionally uses lectures on subject matter and is supplemented by laboratory experience. If the laboratory experiments are not generating the expected results, very often the whole experiment needs to be repeated. The unexpected results could be due to faulty components, incorrect design specifications, or improper connections. Nonetheless, implementing a circuit in the lab with undesired output might be time consuming. However, having an electronics simulator will enable the students as well as the instructor to analyze the performance of a circuit prior to implementing the actual hardware components.

This paper investigates design, simulation and implementation of a decade counter using modern computer hardware and software. This effort will focus on developing an integrated solution of a digital electronics project that will be based on a hybrid environment in which the design and experiments will be simulated and tested in virtual as well as with real electronics components. Students' outreach program in this study is to motivate students to enroll in Electronics Engineering Technology program.

Introduction

Traditionally, many institutions world-wide supports the teaching model in which the students learn circuit theory by participating in lectures, and acquire a deeper fundamental understanding through complimentary experiments. The laboratory experiments presents a design challenge that requires students to apply theory from lectures using hand calculations, create and measure their designs, and then compare their results with the expected values [3]. However, these laboratory experiments are costly, time-consuming, and complicated to schedule.

With the progression in computer technology several electronics laboratory simulation software packages are available to academia and industry. The Multisim® software developed by the Electronics Workbench and National Instruments is a popular circuit capture and simulation software that is frequently used for education and training. With power and flexibility provided by Multisim® students gain the advantages of an industry-caliber, easy-to-use circuit simulator. Multisim® includes powerful virtual instruments, which are simulated instruments found in the laboratory such as oscilloscopes, multimeters, and function generators, among many others. These instruments provide students with a fast and intuitive method for obtaining simulation results while preparing them for the instruments they will use in the laboratory.
Multisim® provides the integrated platform which provides an uninterrupted flow of data from simulation to prototyping and measurement, bridging the gap between theory and hands-on learning. This platform will allow students quick and easy access to measurements. An integrated laboratory presents a unified platform for simulation, prototyping, measurement and

comparison. With a consistent approach and the power of computer-based measurement, students will quickly and easily understand how to implement their design, carry out powerful simulations, and take important measurements. A conceptual view of the integrated platform is shown in Figure 1.

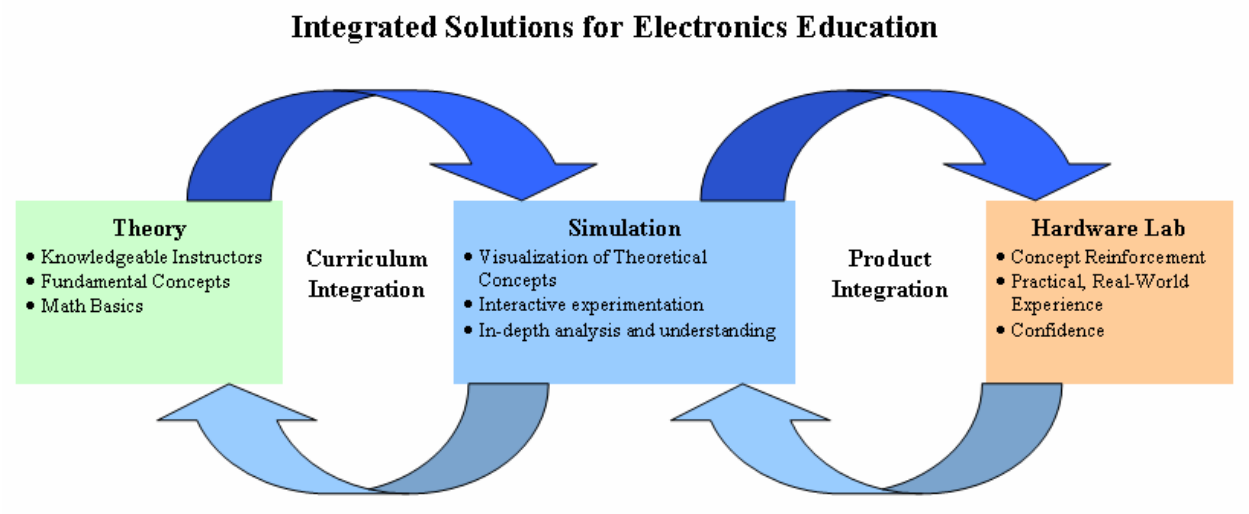

Figure 1: A conceptual view of Integrated Platform

This paper explores the hardware design and software simulation of a decade counter. Design experience included sequential design concepts, selection of components, and software simulation with Multisim®.

Following paragraphs will describe the sequential design of a decade counter, followed by the traditional and design implementation of the counter. The comparison of traditional and design implementation shows that the worst case timing situation are the counting transition from state 0011 to state 0100 and from state 0111 to state 1000.

Methods (Sequential Design)

The design of a synchronous sequential circuits starts from a set of specifications and culminates in a logic diagram or a list of Boolean functions from which a logic diagram can be obtained. In contrast to a combinational logic, which is fully specified by a truth table, a sequential circuit requires a state table for its specification. Steps for the design of sequential circuits are shown in Figure 2.

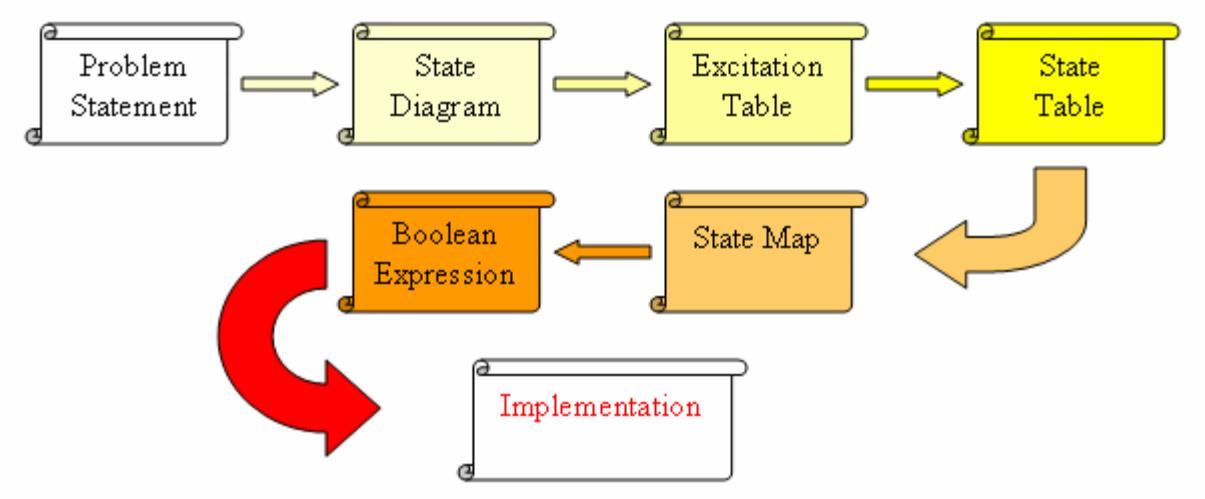

Figure 2: Steps for the Design of Sequential Circuits

A synchronous sequential circuit is made of flip-flops and combinational gates. The design of the circuit consists of choosing the flip-flops and then finding the combinational structure which, together with the flip-flops, produces a circuit that fulfils the required specifications. The number of flip-flops is determined from the number of states needed in the circuit. We wish to design a decade counter whose state diagram is shown in Figure 3.

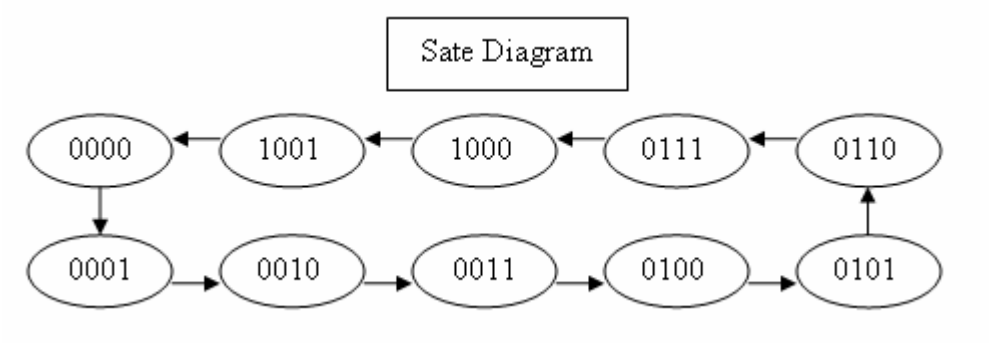

Figure 3: State Diagram for the Decade Counter

The type of flip-flop to be used is J-K. The circuit has no inputs other than the clock pulse and no outputs other than its internal state. The next state of the counter depends entirely on its present state, and the state transition occurs every time the clock pulse occurs. Once the sequential circuit is defined by the state diagram, the next step is to obtain the next-state table, which is derived from the state diagram in figure 3 and is shown in Table 1.

Table 1.0: Next State Table

Present State	Next State
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	0000

Since there are ten states, the number of flip-flops required would be four. Now we want to implement the counter design using JK flip-flops. Next step is to develop an excitation table from the state table, which is shown in Table 2.

Table 2.0: Excitation Table

Present State	Next State	J_3 K_3	J_2 K_2	J_1 K_1	J_0 K_0
0000	0001	0 X	0 X	0 X	1 X
0001	0010	0 X	0 X	1 X	X 1
0010	0011	0 X	0 X	X 0	1 X
0011	0100	0 X	1 X	X 1	X 1
0100	0101	0 X	X 0	0 X	1 X
0101	0110	0 X	X 0	1 X	X 1
0110	0111	0 X	X 0	X 0	1 X
0111	1000	1 X	X 1	X 1	X 1
1000	1001	X 0	0 X	0 X	1 X
1001	0000	X 1	0 X	0 X	X 1

Now transfer the JK states of the flip-flop inputs from the excitation table to Karnaugh maps to derive a simplified Boolean expression for each flip-flop. This is shown in Figure 4. The 1s in the Karnaugh maps of figure 4 are grouped with “don’t cares” and the following expressions for the J and K inputs of each flip-flop are obtained:

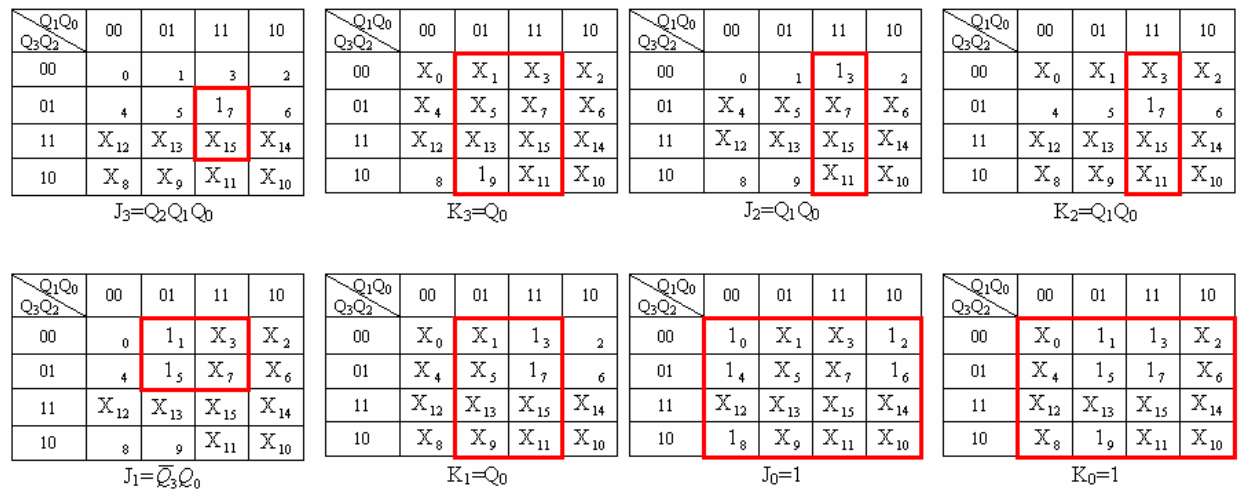

Figure 4: Karnaugh Map

The final step is to implement the combinational logic from the equations and connect the flip-flops to form the sequential circuit. Multisim was used to simulate the designed sequential circuit. Simulation diagram is shown in Figure 5.

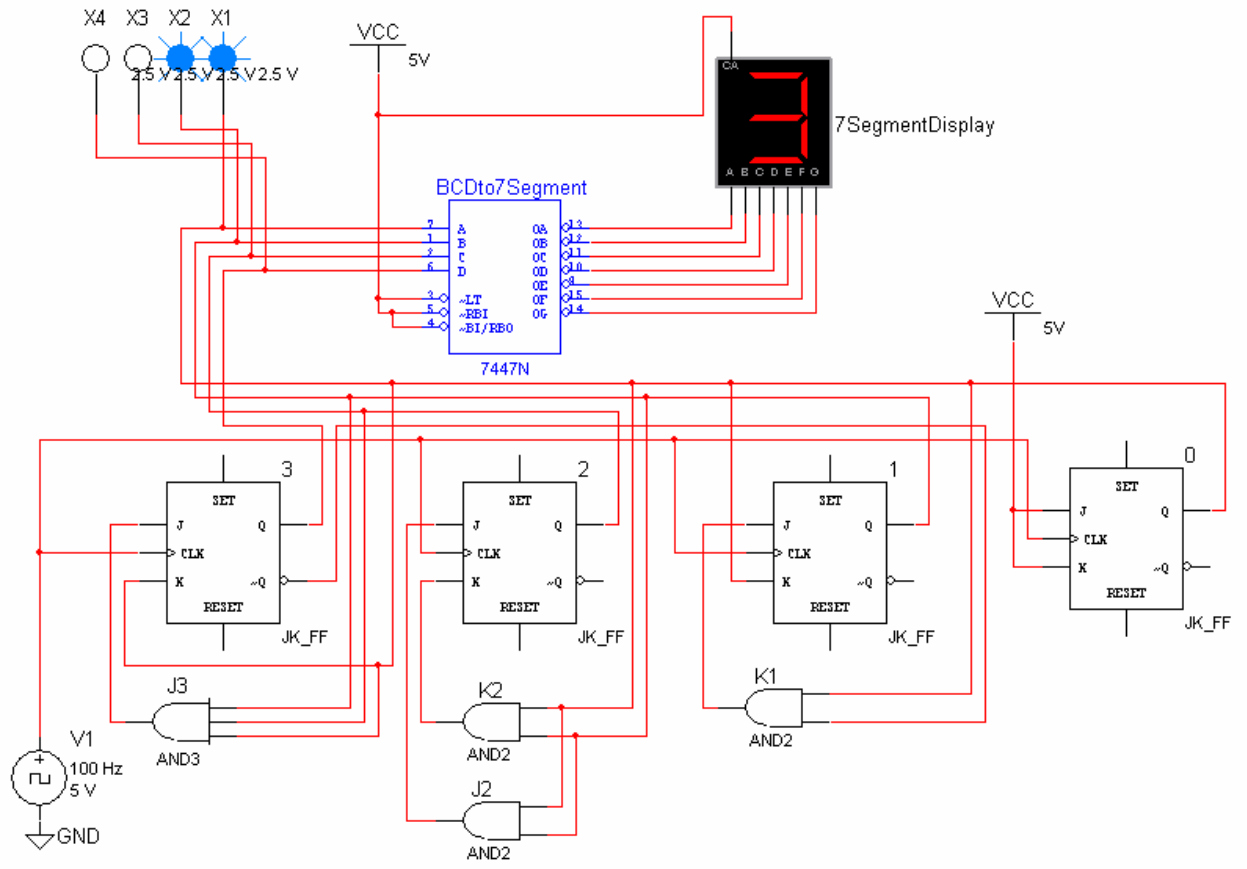

Figure 5: Simulation of the design of decade counter

Schematic of a decade counter using the 7490, 7447 (decoder driver), and 7- segment display is shown in figure 6. Close analysis of both the design and standard chip implementation indicates that the worst case timing situations are counting transition from state 0011 to state 0100, and from state 0111 to state 1000.

Next section will discuss the work conducted by Luiz Carolos Kertly and Daniel Cardoso de Souza [4] to resolve the timing issues. The authors have suggested for transitions to properly occur, the added propagation delays in FF1, FF2, and FF3 have to be less than half the period of the clock signal. For the first transition, after the negative clock edge, propagation time delay of FF1 passes until QA goes down, then one more time propagation time delay of FF2 passes until QB goes down, and finally one more time propagation time delay of FF3 for QC to rise. For counter operation at a 1GHz clock frequency, $t_{PD, FF1} + t_{PD, FF2} + t_{PD, FF3} <= 500ps,$ which means that the t_{PD} of each FF must be less than approximately 160ps [6].

First, one FF must be designed to meet this timing constraint, while also showing an acceptable Vpp with a realistic tool load; then, after this compliant FF cell has been simulated and found to be adequate, it will be used as a reference point in addressing the decade counter problem. The study conducted by Luiz et al shows that the flip-flops need to be redesigned at the chip level to achieve better and robust performance of the counter.

The decade counter was also simulated using NI-ELVIS [5]. The step up of the counter and NI-ELVIS interface is shown in Figure 6. The timing diagram analysis also shows that the transition of the counter is not smooth from the states 0 to 3 and 7 to 8.

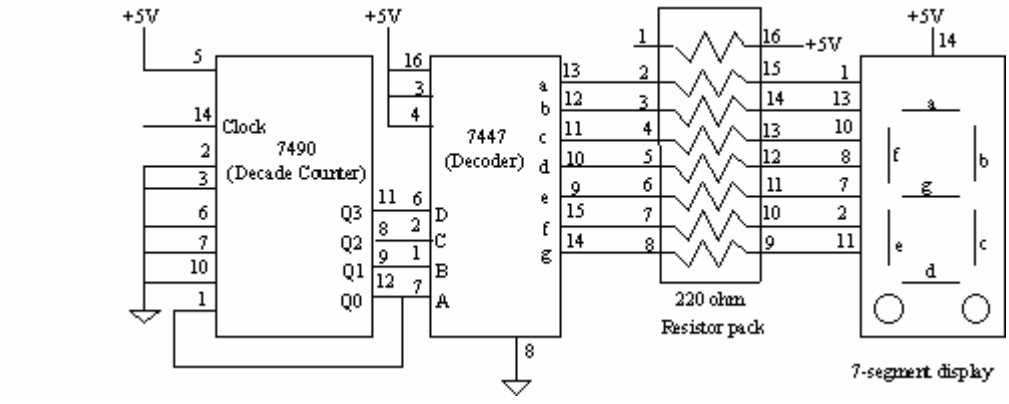

Figure 6: Decade counter with off the shelf chips

Figure 6: NI -ELVIS and Decade Counter Interface

Student Outreach Program

The project offered an opportunity for students to work with others in their class whom they had never worked with. This activity focused on important learning concepts such as Electronics, Programming, Teamwork, and Cross Disciplinary Interaction.

Electronics symbolize the interrelationship between various substructures of the circuit. This includes an understanding of electronic components and the manner in which all these components function together as a deterministic whole system. Basic components such as flip-flops, displays, counters and electronics which include NI-ELVIS, and the Multisim system are the major components of the project activity. Integrating these components offered an opportunity for the students to understand the design/development of digital systems.

Programming varied from high school students to college students. The high school level students were trained to program the circuit from the user end point of view. At college level the students were introduced to design concepts.

The project carried out the concept of teamwork in all phases of design and implementation. The goal of linking the students into a learning community is to give the student a peer group in which they feel comfortable. The team work prepares the students to solve technical problems in a group environment in addition to meet new challenges encountered in the work place. Students experience being on successful teams to appreciate and understand the value of good team work. The project emphasizes on the word team because team is not same as group. The term group implies a somewhat more than a collection of individuals but the team implies much more [2].

The curriculum in any specific area of study tends to narrowly focus students on that area, whereas real-world multifaceted systems tend to incorporate components from multiple disciplines. The development of such systems has shifted from designing individual components in segregation to working in cross-functional teams that include the variety of proficiencies needed to design an entire system [1].The counter design provides an opportunity for students interested in electronics, design, application and troubleshooting to combine their interest in building a digital systems project..

The goal of this outreach program was to exemplify the impact of design and implementation of digital systems in learning Mathematics and Science at the secondary school level. Significant trends were measured from the activity which included the Electronics, Programming, Teamwork, and cross disciplinary interaction. The results show that the students learned tangible lessons from each topic.

Results

The design and implementation of the decade counter was completed. The simulation analysis of the decade counter using the Mutlisim revealed that the worst case timing situations were from counting transition from state 0011 to state 0100, and from state 0111 to state 1000. VI was developed using LabView to acquire data from the decade counter circuit built on NI-ELVIS. It was observed that for the transitions to occur properly, the added propagation delays in FF1, FF2, and FF3 have to be less than half the period of the clock signal. Final analysis of this case study revealed that the redesign of the flip-flop is required for counter to work properly. However, testing of the circuit board under actual working was successful. The circuit was constructed on NI-ELVIS and the tests were successful and the checks were correctly performed.

Conclusion

The project was a successful collaboration between the faculty of SSU and GTREP students at SSU. The designed unit met expectations of the circuit performance. The students had an opportunity to work on a project that involved design and implementation of digital systems. The students will also assist the faculty to promote the design and application concepts to the high school and college students which will serve as a model for improving and creating interest in Engineering and Technology education.

Acknowledgements

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References

[1] Aldridge, M.D. (1996) *Cross-Disciplinary Teaming and Design* (ASEE Annual Conference and Exposition, 1996.)

[2] Courtner, Lyons, Millar, and Bailey (1999) *Student Outcomes and Experiences in a Freshman Engineering Design Course.* (1999 ASEE Annual Conference and Exposition, session 2553)

[3] Evan, Robinson (June 2006). *An Integrated Platform for Electronics Education: A Case Study*.

[4] Luiz, Carolos Kertly & Daniel, Cardoso de Souza. *Design of a "7490-Like" Decade-Counter Integrated Circuit, Using GaAs MESFET DCFL Family, for Frequencies up to 1GHz.*

[5] National Instruments *NI-ELVIS*. Dallas, TX.

[6] Vitesse Semiconductor Corp (1993) *"Foundry Design Manual"* (Version 6.0).