Computer Aided Design of Internally Compensated CMOS Operational Amplifiers

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Abstract - In this paper a design procedure and successful experimental results obtained from it are being reported for implementing internally compensated operational amplifiers powered from a single power supply and with high gain-bandwidth product, good slew-rate, low output impedance and good drive levels. The procedure was developed for an in-house training course on "analog integrated circuit design" as an example of using mathematical tools (MathCad) in the design of analog integrated circuit blocks. The resulting MathCad file became a design automation tool for CMOS OpAmp Design. It is shown that all opamp specs targeted are met or exceeded by the sample opamp designed and fabricated using Fairchild Semiconductor's CS80C CMOS process with the W/L ratios predicted by this tool.

1. Introduction

In the design of electronic circuits, in particular, those falling within the classification "Analog" lack of design automation tools results in over reliance on engineering intuition and experience, and time consuming trial and error method to make the circuit "work". The more complex the circuit, and the less experience and intuition the designer has, the more the time spent becomes on trial and error runs simulating and re-simulating to find an acceptable solution. In many instances this is a justified method, because of non-linear and mathematically difficult nature of the electronic circuit design problems. However, just like in the solution of simultaneous nonlinear equations, if initial guesses are far away from the true solution, at some point the designer may face the frustrating and embarrassing situation that the trial and error method stops improving the performance and the required specs cannot be met. In order to minimize the time needed for trial and error period initial design results should be as close to the solution as possible.

In this work, design, fabrication and testing of an internally compensated CMOS operational amplifier was done complete with its reference bias current source and internal capacitor. The work was done as an example in the CMOS Analog training class taught by M.G. Guvench at Fairchild Semiconductor's Product Development Center. A MathCad file developed by the instructor was used as a design automation tool to calculate W and L parameters of all of the transistors in the circuit as well as resistors and frequency compensation capacitor in a PMOS input CMOS operational amplifier circuit.

2. Design and Fabrication

Design specifications were chosen to create a realistic device whose specifications match or exceed a competitor's product, namely Texas Instruments' TLV2332 CMOS Operational Amplifier.[7], and yet generic enough to be employed as an on-chip operational amplifier in the new analog and mixed-signal products to help with bias and temperature stability, to build active filters, and other uses. For this second purpose, single and low power supply operation, high differential gain, low offset voltage and low power consumption become the primary design goals.

Fairchild Semiconductor's "CS80C" generic CMOS process was chosen to make it compatible with most mixed-signal designs which do not require the options available in its more expensive BiCMOS version, "CS80Cbi". In the absence of Poly1-Poly2 capacitor option, the on-chip frequency compensation capacitor had to be built creatively by employing the Metal1-Metal2 and Poly-Metal1 parasitic capacitances by constructing a Poly-Metal1-Metal2 sandwich structure which forms a shielded Metal1 capacitor.
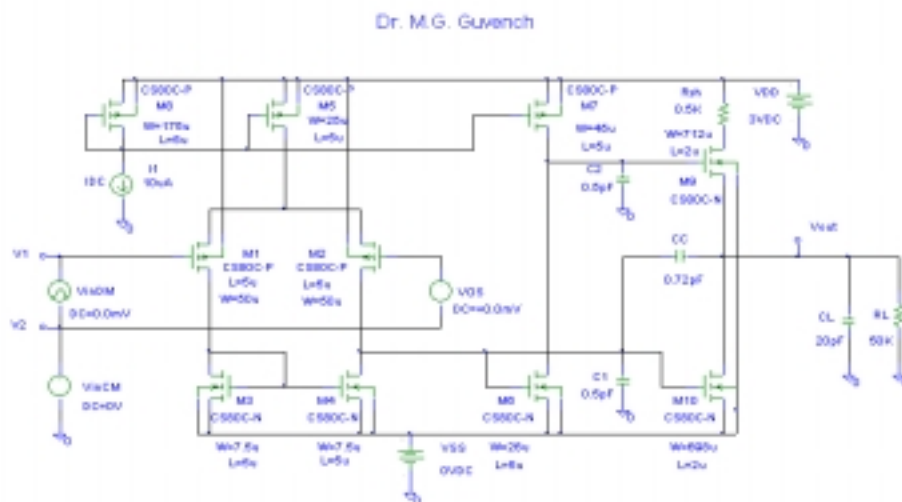

Figure 1. Schematic Diagram of the OpAmp

The opamp's circuit diagram is shown in Figure 1. It comprises of three stages, (1) a PMOS input differential amplifier for low noise, and for a common-mode input range that covers the negative rail (or ground) for single power supply operation, (2) an NMOS common-source high gain middle stage, and (3) an NMOS source-follower output stage for low output impedance and high current. It employs Miller capacitance frequency compensation technique. However, unlike the traditional connection (see Refs. [1,2,3]) of the compensation capacitor, CC which goes across the second stage, in this circuit CC is connected across the input of the second stage and the output of the third. By including the source-follower output stage as unidirectional buffer feed forwarding and the zero introduced by feed-forwarding is eliminated. Thus, the source follower is made to serve both for buffering the output and for internal frequency compensation, as well.

The circuit is biased by a 10μA current source implemented as a beta-multiplier [2]. This bias current reference, I1= 10 μA is cloned into individual stage bias currents as it passes through the current mirrors (M8, M5, M7) and (M4, M10) into all three stages of the operational amplifier to create tracking bias currents. Since the open-loop gain, the gain-bandwidth product and the output drive current directly depend on the drain bias currents of the active transistors in the circuit, this interdependence can be used to program the specs of the opamp via an externally supplied current if needed.

Equations giving bias and device dependent relationships of CMOS amplifiers can be found in texts listed in the References section of the paper [1,2,3]. The design procedure should employ these quantitative relationships and add assumptions, restrictions, limitations and accurately determined device model parameters so as to be able to calculate the sizes of the devices. For a given set of power supply voltage, maximum output swing, minimum acceptable slew rate, voltage gain and gain-bandwidth product values specified, the MathCad program calculates the dimensions of all of the transistors and size of the compensating capacitor. It also predicts the common-mode range, common-mode-rejection-ratio and the power supply current of the circuit. The design equations used are based on the analytical square-law model of the MOSFET , similar to the Spice Level2 model. Therefore, the program works seamlessly with Spice level2 model parameters. However, if more accurate Bsim3 models are available instead the model parameters have to be passed through a translation/interpretation step [2]. Fairchild's CS80C processed devices are characterized in Bsim3, therefore a second version of the program including such translation/conversion steps had to be written.

Because of limited space, the MathCad program named "OpAmp-Design.mcd", or its Bsim3 enhanced version are not being included in this paper. However, interested readers may request a copy from the author (see References [9]).

3. Test and Measurement Results

The design was put into Spice simulation tests thoroughly. Open loop DC tests were employed to check for output drive levels, differential gain, input offset voltage and common mode range under varied temperature (-40C to +85C) and VDD supply voltage steps (2V, 3V, 4V, 5V and 6VDC). Once input offset voltages were ascertained, after proper bias for offset correction is applied, Spice AC test simulations were run to determine the frequency response, gain and phase, of the operational amplifiers. With Fairchild's 0.8μ gate CS80C process gain bandwidth products of several MHz were easily reached with the design criterion of 60° phase margin. Spice transient simulations on the circuit yielded good slew rates (1V/μs).

The Spice simulation of the operational amplifier were done on both a PC running Microsim's version 8 and also on a Sun station running Cadence suite, namely Analog Artist v.4.4.3. It was determined that the differences in the results were insignificant. After this thorough design verification of the opamp and also the peripheral circuits designed for biasing it, layout designs were generated using Fairchild's CS80C process parametrized component library and Cadence suite. The resulting experimental chip whose name "OpAmp1" reflects the fact that it is a

candidate to become the first CMOS operational amplifier in Fairchild Products list came out from the fab recently. The 20-pin chip contains two current sources, one "beta-multiplier" and one "Vt-reference" and two test capacitors in addition to the three opamps designed each with some variation in the design specs. In the experimental data presented below the opamps were biased by the beta-multiplier circuit built on the same chip by simply connecting opamp bias terminal to the beta multiplier reference output.
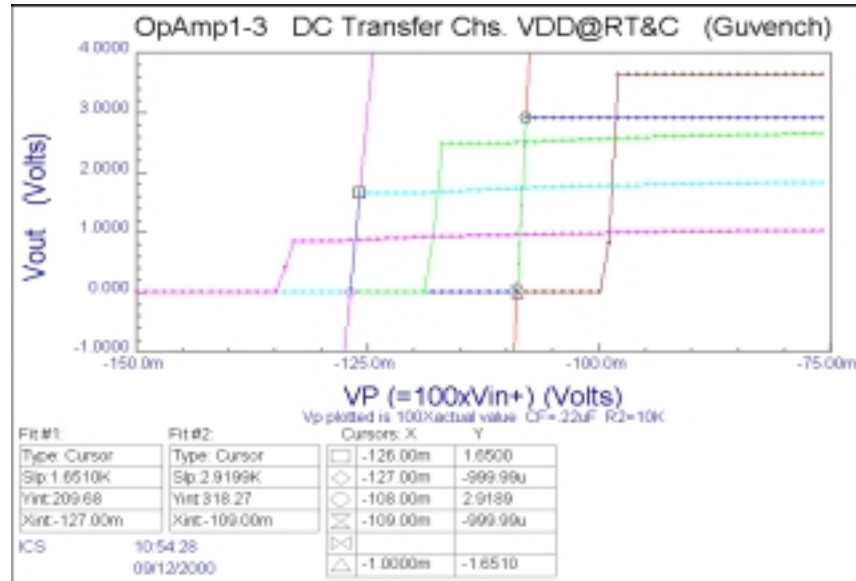

Figure 2. Open-loop DC Transfer Characteristics Measured at VDD= 2V, 3V, 4V, 5V and 6V.
(Note 100 times expansion in x-axis scale, i.e. true x-axis voltage is 100x smaller than shown.)

Figure 2 shows open-loop DC transfer characteristics of OpAmp1 measured under different VDD supply voltages. Open-loop gain and input offset voltages extracted from the DC transfer characteristics are 165,100 and -1.27mV for VDD=3VDC and 291,990 and -1.09mV for VDD=5VDC, respectively. This measurement was done using a HP4145 Semiconductor Device Analyzer GPIB interfaced to a Pentium PC and driven by ICS software. In order to achieve $10\mu V$ step resolution mandated by the very high gain of the sample, HP4145's voltage was applied to the opamp's input after a voltage reduction of 100x via a resistive voltage divider. The horizontal voltage axis shown in Figure 2 shows HP4145's output, therefore, true voltage applied to the opamp's input has to be found by dividing it by 100x.

In the measurement of open-loop DC characteristics of high gain opamps, even though internally frequency compensated, the high differential gain of the amplifier coupled with parasitic capacitances can easily create conditions of instability and oscillations. A high-pass RC feedback from the output terminal to the inverting input, while not interfering with DC measurements, helps to suppress positive feedback and any potential oscillation due to it.

The frequency response characteristics of the operational amplifier are shown above in Figure 3. Both gain and phase plots are drawn using the same frequency axis. In this case the opamp was connected as a 100 gain amplifier to avoid parasitic oscillations under open loop high-gain

conditions. From the gain plot it is obvious that a single pole dominates the frequency response over the useful (gainful) range of frequencies (up to about 5MHz) with a constant roll off of -20dB/decade. The gain curve hits 0 dB at about 2.3 MHz, implying the unity gain frequency (or GBW product) of the opamp to be as high as 2.3 MHz. At that frequency the phase plot shows a phase value of about -130°, implying the opamp is quite stable with a phase margin of 50°. These measurements were done using a home-made automated frequency measurement system described in Reference [6]. Scattered appearance of the data points above 5 MHz is due to noise limitations of the measurement setup.
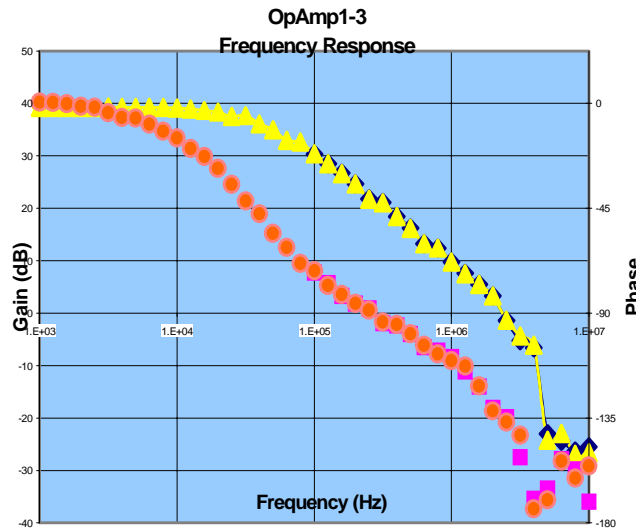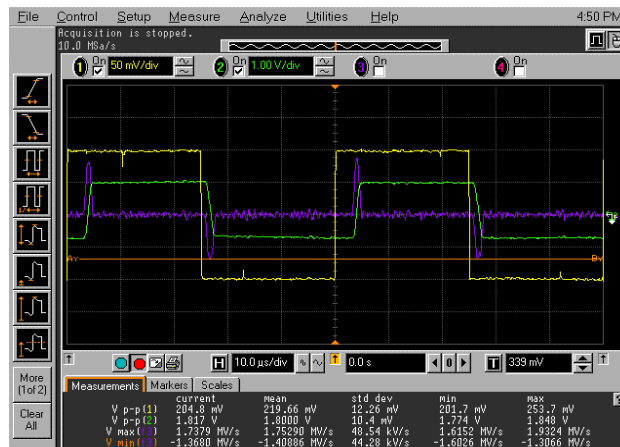

Figure 3. Frequency Response of OpAmp1-3

Figure 4. Slew Rate Test

Slew rate tests done on the operational amplifier (see Figure 4) have shown that the opamp can deliver about +1.7 V/μs and -1.4V/μs. In Figure 4 the narrow pulses (purple) coinciding with

the edges of the green (opamp output wave) are actually the time derivative of the opamp output, therefore the narrow pulses' heights display the slew rate (dV/dt) directly.
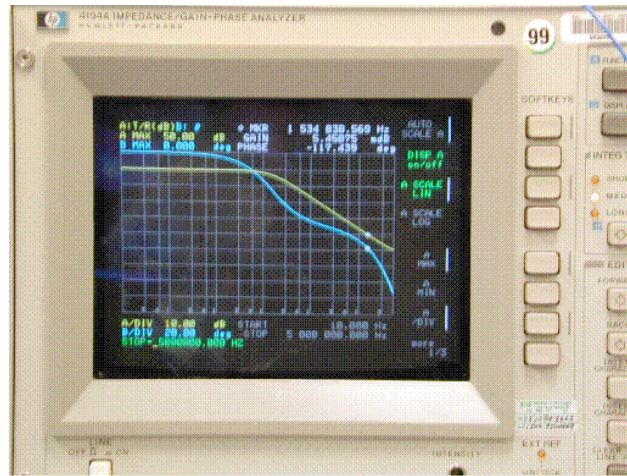

Figure 5. Frequency Response of A PMOS Input OpAmp Designed and Fabricated Using MOSIS 2 micron N-well technology

4. Conclusions

Measurements done on OpAmp1 chip showed that we have matched or exceeded TI's TLV 2332 (an arbitrary reference picked at the beginning) in the power supply and temperature ranges of, $2V < VDD < 6V$; $-40C < T < +85C$ with $I(VDD) < 300uA$, Voffset ~ 1mV, Gain > 100,000, $VOH > 3.5V$ @ VDD=5V and $VOH > 1.8V$ @VDD=3V, Slew Rate > 0.5 V/us and GBW > 0.5MHz @ VDD=5V and GBW > 0.3MHz @VDD=3V.

Experimental verification of the design procedure and the success obtained has resulted in the utilization of this operational amplifier as a building block in other designs. Already opamp1 reported here has found its application in implementing VDD and temperature independent VCO design for PLL applications, band-gap reference and constant current modules.

The same design procedure has also resulted in successful OpAmp designs with both NMOS and PMOS input versions using MOSIS 2-micron N-well CMOS technology. This latter technology is used by the author in his "ELE 444 Analog VLSI Design" course at the University of Southern Maine for teaching. Figure 5 is displaying the frequency response (both phase and magnitude), on a recently acquired HP 4194A Gain-Phase Analyser, of a sample PMOS input OpAmp designed by the author as an example for class use. This OpAmp, as observed from the screen shot, yielded 63 degree phase margin at 1.26 MHz unity gain frequency. In the presentation, an example of the OpAmp design procedure and calculations will be demonstrated using the MathCad file developed. (see Reference [9])

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