AC 2012-3651: FROM THEORY TO IMPLEMENTATION: MEETING INDUSTRY NEEDS THROUGH UNIVERSITY AND COMMUNITY COLLEGE COLLABORATION IN DIGITAL LOGIC DESIGN

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From Theory to Implementation: Meeting Industry Needs through University & Community College Collaboration in Digital Logic Design

Abstract

Hardware Description Language and Field Programmable Gate Array (FPGA) have revolutionized the way Digital Logic Design is taught and implemented. Traditional ways of teaching logic design using discrete components (TTL: Transistor-Transistor Logic and CMOS: Complementary Metal Oxide Semiconductors) have been replaced by Programmable Logic Devices (CPLD: Complex Programmable Logic Devices and FPGA). Today, a more standard development process is widely used in industry. The process uses Hardware Description Languages as a design entry to describe the digital systems. The two most widely used Hardware Description Languages in industry are VHDL (Very High Speed Integrated Circuit Hardware Description Language) and Verilog (Verifying Logic). Although most traditional electrical and computer engineering programs have updated their curriculum to include topics in hardware description language and programmable logic design (FPGA/CPLD), two-year and four-year electrical engineering technology programs have fallen behind and are moving slowly in updating their curriculum. A survey of 107 two-year electrical engineering technology programs and 52 four-year electrical engineering technology programs showed that only 16.5% of two-year and only 19.5 % of four-year programs in electrical and computer engineering technology at US academic institutions currently have a curriculum component in hardware description language and programmable logic design [3]. Clearly, electrical engineering technology programs are far behind in teaching the skills that represent current and future industry needs. As a result, the School of Technology at Michigan Tech University in partnership with the Community College are stepping up to this challenge by developing and introducing curriculum in hardware description languages and programmable logic design. This paper will discuss the curriculum development at Michigan Tech Electrical Engineering Technology Program by incorporating the two courses in logic design and hardware modeling using VHDL and Field Programmable Gate Array (FPGA) Logic Design. The paper will also present the latest National Science Foundation- Advanced Technological Education grant project activities including the Employer Survey to assess the project needs, the faculty workshop training opportunity for interested faculty members at similar institutions, and finally, the undergraduate research experience at Michigan Tech University.

I. Introduction

Programmable Logic Devices in general and FPGA-based re-programmable logic design became more attractive as a design media during the last decade, and as a result, industrial use of FPGA in digital logic design is increasing rapidly. Considering the following technology trend in industry, the need for highly qualified logic designers with FPGA expertise is increasing rapidly. According to the United States Department of Labor, the job outlook is on the rise and will continue to expand for at least the short- to medium-term future [7]. To respond to the industry needs for FPGA design skills, universities are updating their curriculum with courses in hardware description languages and programmable logic design. Although most traditional electrical and computer engineering programs have updated their curriculum to include topics in

hardware description language and programmable logic design (FPGA/CPLD), only 19.5 % of 4-year and 16.5 % of 2-year electrical and computer engineering technology programs at US academic institutions currently have a curriculum component in hardware description language and programmable logic design [3]. To effectively meet the next generation's workforce needs, the electrical and computer engineering technology curriculum must be current, relevant, and teach technology that is widely used in industry. To meet this goal, we propose a curriculum development in the electrical engineering technology program digital logic design series This curriculum revision incorporates the addition of two new courses that added to the current course (Digital Electronics). As a result, the EET program introduced two new courses (Digital Design Using VHDL and Topics in Programmable Logic). Each of these courses is three credit hours (2 class, 3 lab). Faculty involved in developing and teaching the new curriculum must be well-informed of advances in technology currently used in industry. Likewise, industry wants to have qualified and well-educated employees coming out of academia who are ready to implement their knowledge on day one of their employment. As a result, while academia needs to be fully aware of the current state-of-the-art knowledge requirements, industry must be driving the curriculum development. Therefore, in this curriculum development, a strong link between academia and industry must be established. This partnership is a "two-way street" and advantageous for both parties. The Electrical Engineering Technology (EET) program in the School of Technology at UNIVERSITY is collaborating with Altera University program in which the involved faculty members attend a set of Altera training workshops. These workshops are targeted toward professional individuals and college faculty seeking knowledge and expertise in programmable logic design. Faculty members having the opportunity to attend these workshops gain the knowledge and expertise to teach both VHDL digital Design and Programmable Logic (FPGA) design courses. The exposure to industry-taught courses will help the faculty members to impact the learning experience of his/her undergraduate students by providing them with skills that are highly marketable and appreciated by industry.

II. Curriculum Development at Michigan Tech University

Figure 1 shows the current and proposed digital design logic sequence which incorporates the addition of two new courses that will be added to the current course (Digital Electronics). The EET program will introduce two new courses (Digital Design Using VHDL and Topics in Programmable Logic). Each of these courses is three credit hours (2 class, 3 lab). The descriptions of the two new courses are provided below. We are able to add the two new courses without impacting the overall degree plan. The current EET program has a shortage of courses in digital logic design; only one course (Digital Electronics) is currently offered. The EET program will still be structured as a 127 credit hour program with sixty-eight (68) credits of technical courses in Electrical Engineering Technology. This is in line with ABET requirements [8]. ABET Criterion **5. Curriculum: "**Baccalaureate programs must consist of a minimum of 124 semester hours … and the technical content is limited to no more than 2/3 the total credit hours for the program" [8].

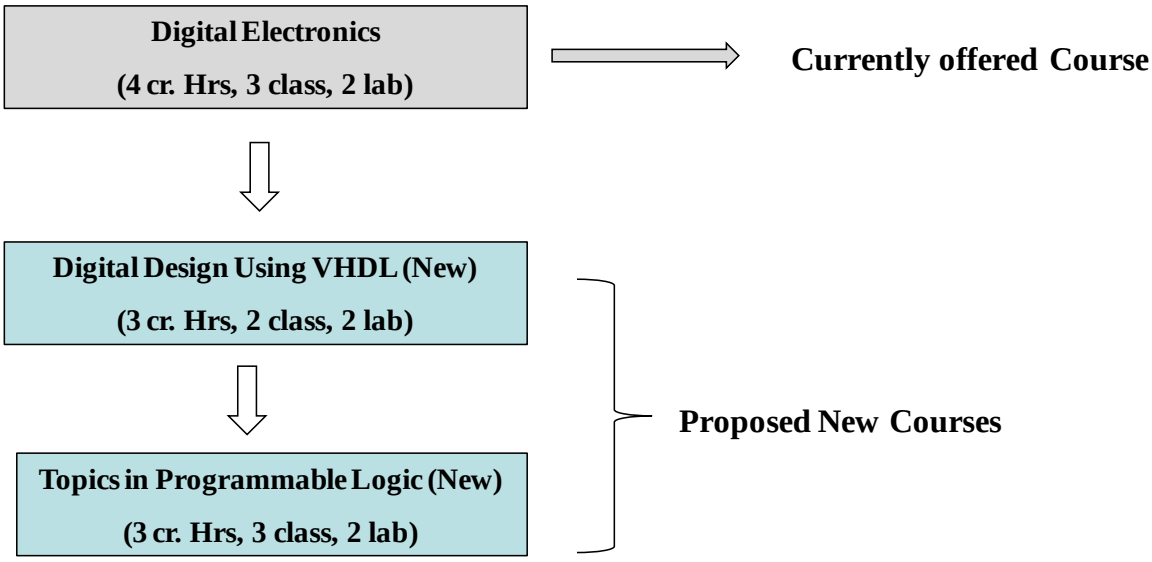

Figure 1: Proposed Digital Logic Design Courses Sequence

<u>New Course 1: Digital Design Using VHDL</u> (3 Cr hrs, Class 2 hrs, Lab 3 hrs)

Course Objectives

The course places an emphasis on the language concepts of digital systems design using Hardware Description Language (VHDL). The course will focus on good digital design practices and writing testbenches for design verification. Low-level gate modeling techniques with varying timing details will be presented, as well as structural level of abstraction for wiring predefined gates and other predefined components. The information gained can be applied to any digital design by using a top-down design approach. Students will gain valuable hands-on experience in writing efficient hardware designs using VHDL and performing high-level HDL simulations.

The academic objectives of the "Digital Design using VHDL" course are to provide students with skills and experience that will help them to be attractive in the job market and as employees with high-value skills in the workplace. The students will learn the design of major components of digital systems, such as arithmetic logic units (ALUs), floating points, memory, and controller using hardware description language (VHDL). In addition, the students will learn FPGA design flow starting from HDL design entry and circuit simulation to verify the correctness of the intended design, writing testbenches. To accomplish this in a one-semester course, the intent of lectures and labs is to have the students:

1. Gain the knowledge on programmable logic devices (PLD) and their design methodologies
2. Learn fundamental concepts of hardware description language
3. Learn how to use HDL for modeling basic building blocks of digital system
4. Learn about different design entry methods
5. Learn how to model digital circuits in hardware description languages
6. Learn how to use VHDL editors, debug designs and perform logic simulation
7. Learn how to use Altera's Quartus® II development software
8. Learn how to perform timing analysis and verification

Course Structure
The course "Digital Design using VHDL" is three credit hours with two hours per week of recitation and three hours per week in the lab. The course will be open for sophomore or higher students and the pre-requisite is "Circuits I" and "Programming Languages". The course will integrate Altera's Quartus® II development software, and the lab will use Altera's DE2 FPGA evaluation board.

The first class in VHDL was developed and conducted in spring 2011 with a total of 23 enrolled students. As part of the assessment, a course survey was used to obtain student feedback regarding instruction. There are total of twenty questions in the survey: the first eighteen questions are based on best practice and cover not only curriculum but also classroom and lab facilities; the question 19 and 20 are intended to elicit students' feedback on their overall assessment of the instruction. Students were also encouraged to provide written comments to further improve the teaching practice. Students also rated how well the course objectives were achieved on a scale of 1 to 5 with 5 being Strongly Agree and 1 being Strongly Disagree. Table 1 reflects student feedback regarding access to new, effective curriculum modules and labs that more accurately reflect the needs of industry. Overall feedback was extremely positive.

Measurable Outcomes	**Overall Rate**
Students will learn how to model basic digital circuits in hardware description languages.	4.73
Students will learn how to use VHDL to model common digital hardware circuits - combinational and sequential circuits	4.64
Students will learn how to use to use VHDL CAD Tools (editors, debug designs and perform logic simulation).	4.25
Students will learn how to write test benches to verify the design and perform timing analysis of a given design	4.45
Students are more interested in the subject now than they were before they took the class	3.93
The classroom and equipment were adequate to support effective learning	4.14
Instructional resources (textbook, handouts, etc.) furthered learning	4.29
The instructor made students aware of the specific goals of the course	4.36

Table 1: Students' feedback assessment results

<u>New Course 2: Topics in Programmable Logic Design</u> (3 Cr hrs, Class 2 hrs, Lab 3 hrs)

Course Objectives
Due to industry's increased demand for FPGA designers, the intention of this course is to give students real-world experience in FPGA logic design and provide with the necessary training in design tools widely used in industry. Tools used will include Altera's Quartus® II development software and FPGA design implementation on Altera's DE2 FPGA evaluation board. The long-term objective of this course is to provide a learning opportunity that will result in research activities focused on FPGA design. This research will provide more in-depth training for senior students and engage undergraduate students in applied research opportunities.

The academic objectives of the FPGA logic design course are to provide students with skills and experience in the FPGA design process. The students will learn the FPGA design flow using Quartus® II [2] development software to develop an FPGA, starting from HDL design entry, circuit simulation followed by FPGA Synthesis for Altera FPGA devices, Place and Route and timing analysis. To accomplish this in a one-semester course, the intent of lectures and labs is to have the students:

1. Learn how to use HDL for modeling basic building blocks of digital system
2. Learn FPGA technology and the impact of using FPGA in logic design
3. Learn FPGA design flow using Altera's Quartus® II development software
4. Gain FPGA design experience by synthesizing, mapping, and placing and routing a given design on Altera's DE2 FPGA evaluation board
5. Work in groups of two or three and thereby learn how to cooperate in teams
6. Learn to document their results

The designs are carried out using modern computer-aided design (CAD) tools, and the Altera's Quartus® II development software [2]. The final systems will be implemented with state of the art devices such as the Altera FPGA device family and micro-controllers. Altera's DE2 evaluation boards will be used as the target platforms.

Course Structure

The course "Topics in Programmable Logic" is three credit hours with two hours per week of recitation and three hours of lab. The course is open to senior students and the pre-requisite is "Digital Design using VHDL". The course will integrate Altera's Quartus® II development software. The lab will use Altera's DE2 FPGA evaluation board, the FPGA boards will be used as target platforms for lab experiments. Students will learn how to implement a complete system on the FPGA evaluation boards.

Altera Corporation represents a market leader and holds a large market share in programmable logic. Each FPGA vendor development software is device dependent, for example, Altera's Quartus® II development software only targets Altera's device family. Learning Altera's Quartus® II development software will give students the opportunity to learn FPGA design flow using the most widely used tools for FPGA design. At the same time, these skills are largely transferable to other design tools, so students will learn valuable skills useful across industrial platforms.

The first class in VHDL was developed and conducted in fall 2011 with a total of six enrolled students. As part of the course assessment, a course survey was used to obtain student feedback regarding instruction. There are twenty questions on the survey, the first eighteen questions are based on best practice and cover not only curriculum but also classroom and lab facilities. On the other hand, question 19 and 20 are intended to elicit students' feedback on their overall assessment of the instruction. Students are also encouraged to provide written comments to help improvements of the teaching practice.

III. Employer Survey

As part of the project's needs assessment, a survey was sent to the employers who hire program

graduates to assess how well this educational initiative aligns with their current and proposed future human resources needs. This survey was designed to judge the necessity of providing the type of training we are identifying as important. Forty organizations responded to this survey. Overwhelmingly, the survey respondents identified the ability of technicians and technologists to be able to work with FPGAs as a critical skill. Results from the assessment survey showed that almost 80% of the respondents view knowledge of VHDL and FPGA as a critical skill for making a technician more employable and marketable. Table 2 summarizes responses from 40 industrial and governmental organizations who responded to the survey.

Survey Questions	**Overall Rate**
Should technicians have a basic digital logic education? Yes/No	100 % Yes
Would you benefit by having technicians who know VHDL? Yes/No	65% Yes
Would a technician benefit from the skills to design and interface FPGAs? Yes/No	85% Yes
Would a technician be more valuable to your organization if they could work with FPGAs and had a working knowledge of Hard Descriptive Languages (such as VHDL)?	79% Yes

Table 2: Employer Survey results

IV. Faculty Workshop

An integral part of this project is to offer two 2-day workshops for up to 10 faculty members. The workshop is intended for interested electrical engineering technology program faculty. The goal of the workshop is to combine technical information from the vendor training with practical curriculum planning and strategies for developing courses like those developed at Michigan Tech University under this project. The workshop is to be advertised widely, primarily using engineering technology division (ETD) listservs. The participating faculty members will spend approximately four hours learning introductory material on the impact of teaching engineering technology students relevant skills in hardware modeling and FPGA design. In subsequent sessions, the faculty will learn fundamental concepts of hardware description languages and gain knowledge on programmable logic devices (PLD) and their design methodologies. Participating faculty members will tour the Re-configurable Computing Lab and learn more about both the hardware and software necessary to establish a re-configurable lab at their respective institutions. Following the tour of facilities, participants will spend three hours in a hands-on lab experience to practice modeling basic building blocks of digital systems and learn the FPGA design flow starting from HDL design entry and circuit simulation to verifying the correctness of the design. During the second day, faculty participants will spend approximately four hours drafting potential curricular resources to be used at their respective institutions.

The first summer faculty workshop was offered in September 2011, the project PIs conducted an intensive, two-day workshop on VHDL and FPGA design. There was an overwhelming positive response to the opportunity announced on the Electronics Theses and Dissertations (ETD) listserv, which forced The PI to close the registration after only two hours following the announcement. Representatives from seven institutions in six states (Indiana, Illinois, Kentucky, Pennsylvania, Virginia, and Georgia) engaged in the hands-on learning experience, working with both the software and the hardware. The workshop provided faculty members of community colleges and four-year electrical engineering technology programs with the opportunity to expand their expertise in VHDL and FPGA design. The participants will utilize these skills to

develop new courses in digital logic design, using VHDL and FPGA, at their respective institutions.

V. Undergraduate Research Opportunities:

The long-term objective of this project is to provide a learning opportunity at the School of Technology which will result in a research activities focused on FPGA and hardware design modeling. Research experiences will provide more in-depth training for undergraduate senior students. In addition to involving Michigan Tech University undergraduates in research, undergraduate students from partner community colleges can be involved in research at Michigan Tech. The first EET student was hired in summer 2011 as the project's summer intern. He helped with development and delivery of the summer 2011 faculty workshop. He also designed the project web page and he also developed more in-depth expertise in VHDL and FPGA design.

VI. Conclusion

With the demand of skilled FPGA designers on the rise, the objectives of this paper was to present the year project activities including the Employer Survey to assess the project needs, the faculty workshop training opportunity for interested faculty members at similar institutions, and finally, the undergraduate research experience at Michigan Tech University. The goals of this project are to give students of both two-year and four-year Electrical Engineering Technology a real-world experience on FPGA logic design and give them the necessary training with industry widely used design tools. Students of the electrical engineering technology two- and four-year programs will not only gain skills and knowledge that are highly marketable, but also will work with faculty advisors on applied research projects in hardware modeling and programmable logic design.

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