# Integrating professional TCAD simulation tools in undergraduate semiconductor device courses

**Julie Kenrow**
**Department of Electrical and Computer Engineering**
**University of the Pacific, Stockton, California**

Abstract

Semiconductor device theory and IC processing courses are becoming more important in undergraduate electrical engineering curricula due to the fast changing technologies and challenges currently facing the semiconductor industry. However, in recent years many undergraduate EE programs have cut back or discontinued courses in semiconductor devices, solid-state physics and IC processing due to the high operating costs involved in maintaining an IC fabrication laboratory.

We propose using professional Technology CAD (TCAD) simulation tools [1] as a powerful, yet economical aid in teaching undergraduate students about silicon wafer processing, semiconductor device physics, and device operation.

Who uses TCAD?

TCAD simulation tools are widely used throughout the semiconductor industry to speed up and cut the costs of developing new technologies and devices. Since a decade the R&D departments of semiconductor companies have incorporated TCAD in their design process, and recently the manufacturing sector has begun to utilize TCAD as well, e.g., to analyze the impact of IC process variation, and to investigate possible IC process optimizations as well as for yield analysis.

What is TCAD?

Technology CAD (TCAD) refers to using computer simulations to develop and optimize semiconductor processing technologies and devices. TCAD simulation tools solve fundamental, physical partial differential equations, such as diffusion and transport equations for discretized geometries, representing the silicon wafer or the layer system in a semiconductor device. This deep physical approach gives TCAD simulation predictive accuracy. It is therefore possible to substitute TCAD computer simulations for costly and time-consuming test wafer runs when developing and characterizing a new semiconductor device or technology.

TCAD consists of two main branches: process simulation and device simulation. In process simulation, processing steps such as etching, deposition, ion implantation, thermal annealing and oxidation are simulated based on physical equations, which govern the respective processing steps. The simulated part of the silicon wafer is discretized (meshed) and represented as a finite element structure (see figure 1). For example, in the simulation of thermal annealing complex

diffusion equations for each dopant species are solved on this mesh. For oxidation simulations the growth of the silicon oxide is simulated taking into account the oxygen diffusion, the mechanical stresses at corners, etc. In another example, Monte Carlo techniques are often used to simulate the process of ion implantation, where ion-semiconductor interactions are taken into account to compute individual ion paths.
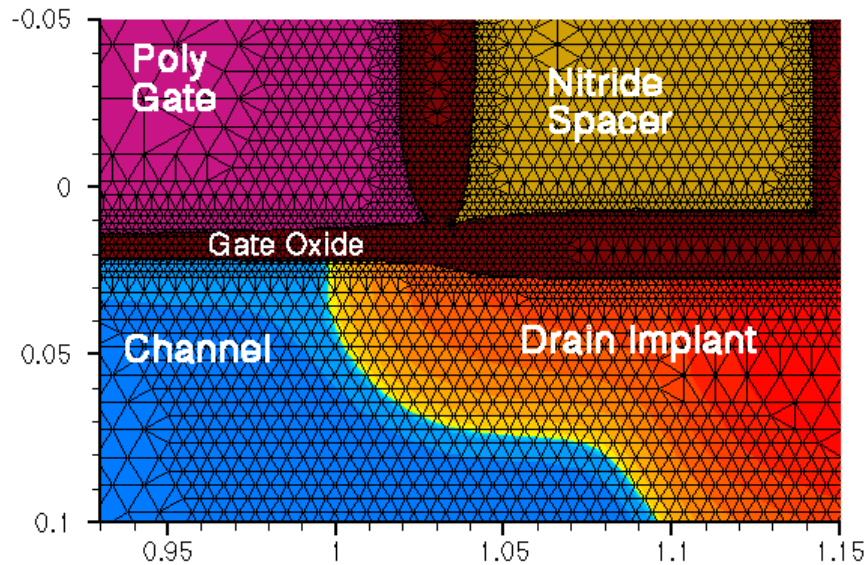


Fig. 1: Close-up of the gate-drain corner of an nMOSFET with finite element grid. TCAD simulators solve physical partial differential equations on a finite element grid representing a discretized model of the physical device.

Device simulations can be thought of as virtual measurements of the electrical behavior of a semiconductor device, such as a transistor, or a diode. Again, the device is represented as a meshed finite element structure. Each node of the device has properties associated with it, such as material type, doping concentration, etc. For each node the carrier concentration, electric field, etc. are computed. Electrodes are represented as areas on which boundary conditions, such as the applied voltage, are imposed. The device simulator solves the Poisson and the carrier continuity equation (and possibly other equations, such as lattice and carrier temperature equations). After solving these equations the resulting electrical currents at the contacts are extracted. In summary, TCAD simulation tools are very powerful and do not rely on simplistic assumptions, but instead solve realistic physical "microscopic" equations.

What does TCAD bring to the undergraduate classroom and laboratory?

1) Visualization

Visualization is one of the big advantages of TCAD tools. During the process simulation the evolution of actual cross-sections of the structure can be seen. For example the detailed process of growing oxide can easily be visualized at any point in time. Such detailed and accurate visualizations can only be obtained with TCAD (see figure 2). Without TCAD the student would have to rely on simple sketches or on STM and TEM micrographs in textbooks (or literature) to understand how a certain processing step changes the structure of the device. Also doping

profiles can be extracted after implantation and after annealing (see figure 3). Such information is otherwise available, again, only as oversimplified sketches or as SIMS profiles reported in textbooks or literature.
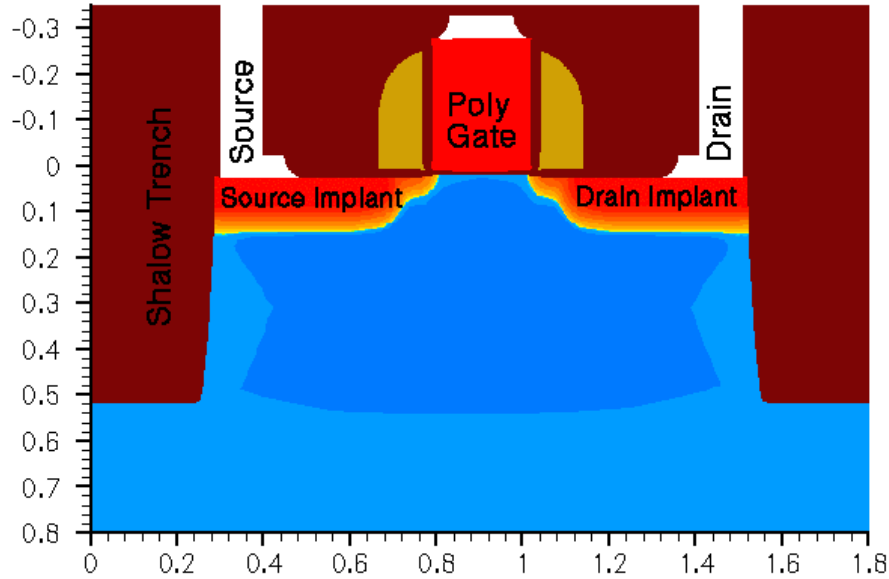


Fig. 2: TCAD for visualization: Cross-section of a 0.25-micron NMOS transistor simulated with the ISE process simulator DIOS. Process flow after Plummer [2].
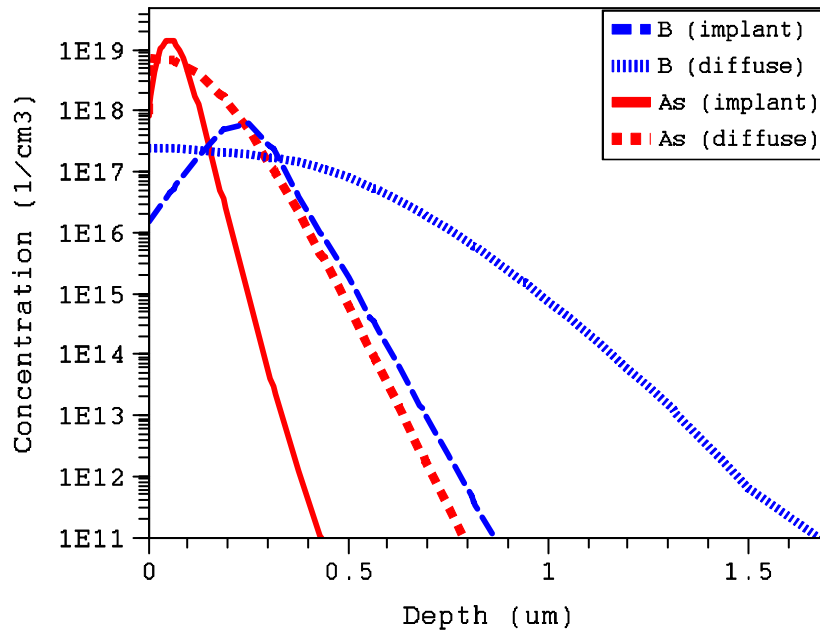


Fig. 3: TCAD for visualization: Arsenic and Boron profiles in a BJT. As implanted profiles and profiles after annealing for 15min at 1100 C. The simulation is performed with DIOS.

For device simulations terminal currents and voltage values, as well as the carrier and current distributions, electrical fields and electrostatic potentials can be visualized for any bias condition anywhere in the device. For example it is possible for a student to observe the formation of the inversion layer in a MOS capacitor, the current flow in a MOSFET device, and carrier recombination in the base and emitter of a BJT. Such visualizations cannot be obtained experimentally. Thus TCAD serves as a "microscope" with quite remarkable capabilities.
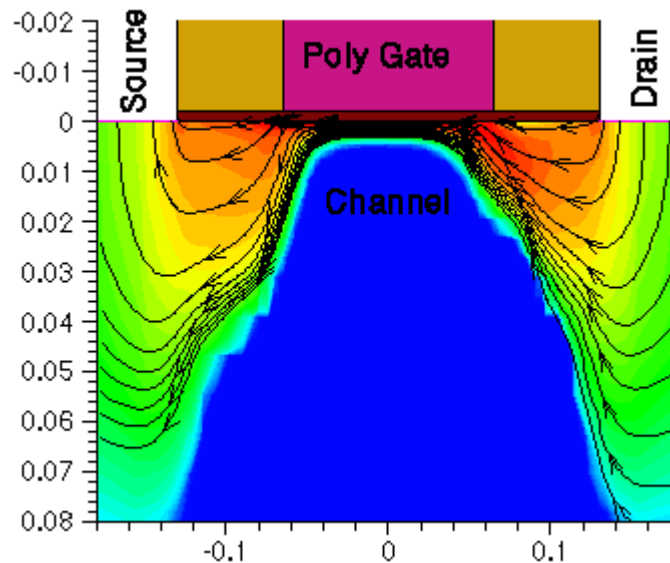


Fig. 3: TCAD for visualization: Current flow lines in a 0.13-micron nMOSFET at Vg=1.5V and Vd=3.0V. The shading represents the current density. The simulation is performed with the ISE device simulator DESSIS.

On the other hand, web-based Java applets such as SIMPLer [3] from the University of California, Berkeley and the applet collection from the "Educational Java Applet Service" at SUNY Buffalo [4] also provide nice illustrations for processing and various device behaviors. However, these applets are based on simplified animated sketches or are derived from 1D models. These popular applets provide a qualitative overview of IC processing and semiconductor device operation, but they do not attempt to describe actuate behaviors. This can only be achieved with TCAD.

TCAD visualization can be brought to the classroom in different ways. Fixed graphics can be integrated into course notes and the evolution of a simulation can be presented as a movie, e.g., embedded in a PowerPoint presentation. In addition, TCAD software (from certain vendors [1]) runs with reasonable speed on any modern laptop under Linux or Windows operating systems, making interactive simulations possible in classroom.

2) Validity of commonly used simplified device models.

In device physics courses many simplified models are introduced, such as the "constant depletion width approximation", the 1D MOS capacitor, and the "MOS Level 1" compact model. These models are very useful, because they allow the student to focus on the main ideas behind device

operation as well as to understand trends in devices, e.g., how does the depletion width in a pn junction change with the doping concentration. However, to be successful as a practicing engineer one also has to understand the limitations of these simplified models. In standard undergraduate classes these issues are discussed, but they tend to remain abstract to the student. TCAD enables the student to explore the validity of these models by comparing the predictions of the simplified models with the results of a TCAD simulation. The student will thus learn what aspect of a simple model can be trusted and when a more detailed analysis may be necessary. This becomes more and more relevant as the simple models become increasingly inadequate for modern device technologies.
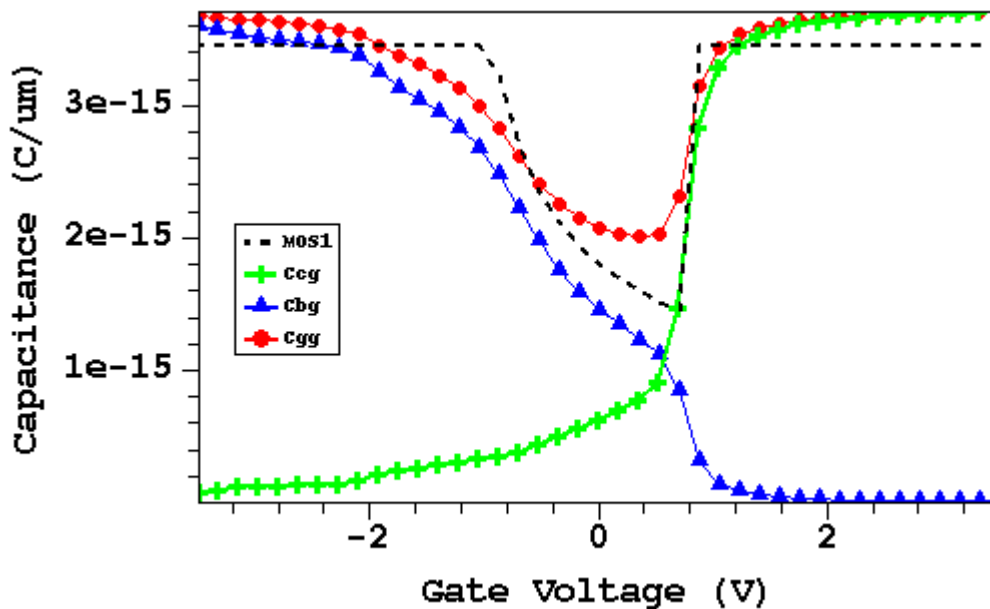


Fig. 4: TCAD for evaluation of simplified models used in class: CV plot simulated with DESSIS for a long channel MOSFET. Circles: Total gate capacitance. Triangles: Gate-source/rain capacitance. Crosses: Gate-body capacitance. Dashed line: Gate capacitance according to the 1D constant depletion width approximation.

A good example is the 1D MOS capacitor. This model is used to explain the formation of the inversion layer in an MOSFET device. While such a 1D model is quite appropriate to describe the long-channel devices of older technologies, modern far sub-micron MOSFETs exhibit strong 2D effects, such as charge sharing between the source and drain depletion regions and the depletion under the gate. Only with TCAD can these effects be visualized and the impact of charge sharing can be discussed in the classroom without burdening the undergraduate student with complex 2D equations.

Another example is the "MOS Level 1" compact model. The student can extract the "MOS Level 1" compact model parameters for a long-channel and for a short channel device from TCAD simulations. Then the student can see, first hand, that the "MOS Level 1" model yields an accurate description for the long channel device, however, it fails to account for high field saturation effects. These effects are quite dominant in short-channel devices and therefore the

"MOS Level 1" compact model leads to an overestimation of the saturation current in short channel devices (see figure 3).

In order to successfully use any model it is essential to understand the difference between the model and "reality", as well as the predictive range of the given model. TCAD may serve as an example of this general concept. For example, in TCAD device simulations, the student can choose between different transport models (drift-diffusion, hydrodynamics, thermodynamics, and quantum transport) as well as different sets of material parameter models (e.g., various mobility degradation or recombination-generation models). From this the student will learn that for certain devices and under certain conditions the inclusion of more refined models may not affect the simulation results and thus simpler models may be sufficient. On the other hand, the student may see that for other devices or under different operating conditions simplified models are not sufficient and more refined models are needed.
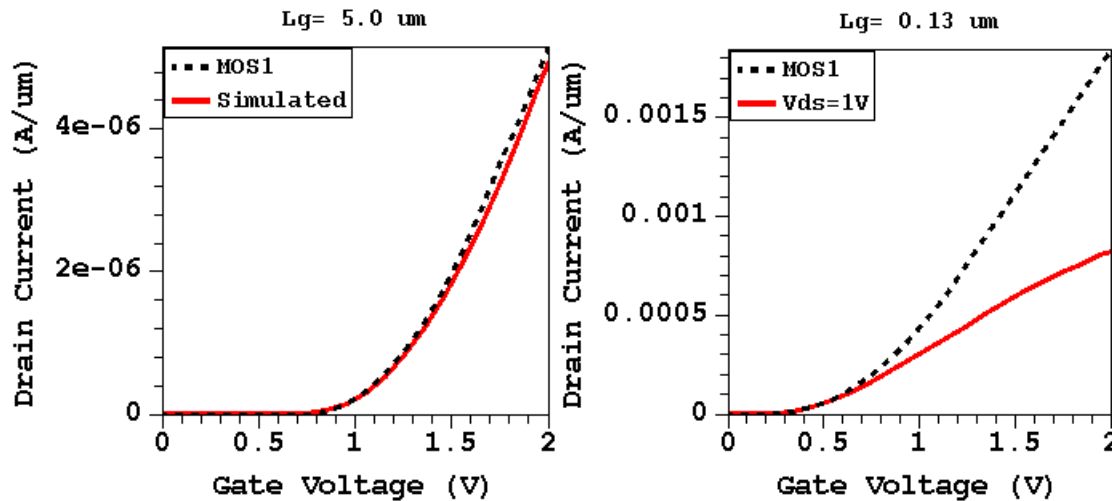


Fig. 5: TCAD for evaluation of simplified models used in class: Comparison of TCAD simulated IdVg curves with the analytic "MOS Level 1" compact model IdVg curve for a 5.0-micron (left) and for a 0.13-micron (right) gate length nMOSFET.

3) "Hands on" experience

Silicon wafer processing is very expensive, and the technology in the semiconductor sector changes so fast that any newly built IC fabrication facility would be relatively obsolete after just a few years. Further, IC fabrication facilities need a considerable number of full time operation personal. As a result, very few universities can afford to maintain an IC fabrication facility. Even then, access a university supported IC fabrication facility is usually limited to a few users, typically graduate students and researchers, due to the high costs of wafers and equipment.

TCAD gives the student, even on the undergraduate level, a chance to learn about realistic silicon wafer processing via hands-on simulation, without the need for IC processing facilities. With TCAD the student can experiment and explore the impact of process flow modifications at

virtually no cost. Powerful computers are readily available on any campus, which the student can access via a computer lab, the library, or even a personal laptop. Although TCAD simulations require considerable amounts of memory and CPU time, recent advances in computer hardware makes even a standard laptop suitable to run realistic TCAD simulations in a matter of minutes.

Laboratory measurements of electronic devices, such as transistors and diodes, are performed easily in student labs and are included in most introductory device labs. However, the selection of commercially available lab chips for testing is very limited and, in fact, decreasing as the number of university IC fabrication facilities is shrinking. In this case, TCAD device simulations can offer a new degree of flexibility. With TCAD the student can perform virtual measurements on a wide variety of devices.
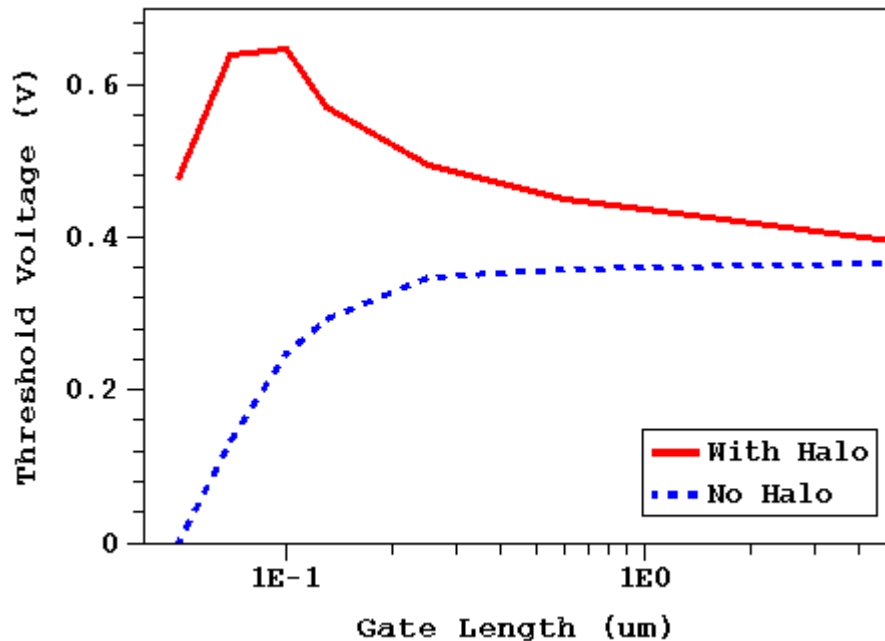


Fig. 6: Threshold voltage as a function of gate length simulated with DESSIS for two slightly different MOSFETs.

Furthermore, TCAD encourages creativity. The interested student can, for example, design, create, and test a device in a matter of minutes to hours, without using expensive and limited resources. Also, TCAD gives the student the opportunity to explore device behavior to a much deeper level. As an example, figure 6 shows the threshold voltage roll-off characteristics of two similar MOSFET structures. By comparing the 2D doping distributions the student can explore how a non-uniform doping distribution in the channel can lead to the "reverse-short-channel" effect.

4) Marketable skills

TCAD simulations are widely used throughout the semiconductor industry. As technologies become more and more complex the semiconductor industry relies increasingly more on TCAD to cut costs and speed up the research and development process. Further, an increasing number of companies are becoming "fabless", i.e., they source out all IC wafer processing to foundries.

As a result fabless IC companies heavily rely on computer simulations to design their products. In addition, semiconductor manufacturing companies use TCAD for monitoring, analyzing and optimizing their IC process flows. The demand for engineers with experience in TCAD is therefore increasing. Possessing a working knowledge or proficiency with TCAD is rapidly becoming a highly marketable skill for IC engineers.

The TCAD learning curve

Professional TCAD simulation tools are in general difficult to use and are considerably more complex than, e.g., SPICE circuit simulators. Ideally, new TCAD users need dedicated training sessions to successfully use the tools. The time necessary to devote for such training sessions is not feasible to incorporate in most undergraduate device courses (unless it is a dedicated elective TCAD course). However, so-called TCAD framework tools, like GENESISe from ISE [1], can overcome this dilemma. GENESISe is a work environment, which creates a user-friendly interface for the TCAD simulation tools. It organizes and maintains simulation projects automatically. GENESISe allows to set-up TCAD simulation projects in a parameterized manner. Within this work environment the student has easy access to certain parameters (predefined by the instructor). For example, the student can modify these parameters and rerun the simulation after reading a brief instruction page. The interested student can always venture beyond the prescribed parameterization to explore the subject at hand to any depth without limits. Some TCAD vendors [1] offer free self-study introductory training material, which the interested student can use. As the student gains more experience with TCAD simulations, lab projects can be defined more freely, i.e., with less parameterization.

An example undergraduate lab sequence based on TCAD

In the Spring of 2003 a new lab sequence based on TCAD was introduced at the University of the Pacific for an undergraduate introductory course in VLSI Design. In the following, a sequence of six TCAD simulation labs, which requires no prior knowledge in TCAD, is introduced.

Lab 1: The student is introduced to the ISE-TCAD framework tool GENESISe. GENESISe is used to structure a simulation project in which the student runs the process simulation tool DIOS to simulate a 0.25-micron technology CMOS process flow [2]. In this lab the student observes the evolution of the device structure through all processing steps and is asked to write down their observations. The final structure is shown in figure 1.

Lab 2: The student explores the layout of a 1-micron CMOS inverter using the layout editor tool PROLYT and then simulates the 1-micron technology process flow [5]. The student compares the process flows for the 1-micron and the 0.25-micron devices. For example, the 1-micron technology uses a LOCOS process for inter-device isolation, while the 0.25-micron technology uses modern "Shallow Trench Isolation". Other process steps to explore are Halo and LDD implants, which are used in the 0.25-micron technology.

Lab 3: The student uses the TCAD tools to design a process flow for a bipolar transistor, using the graphical process flow editor tool LIGAMENT. The student is asked to "reverse engineer" a

BJT given a sketch of the main device cross-section. The student tests the process flow by simulating it with the process simulation tool DIOS and extracting out doping profiles across the emitter-base-collector regions.

Lab 4: The student is introduced to the device simulator DESSIS. The student performs drain current versus gate voltage simulations for a long-channel (5-micron) MOSFET. The gate sweep covers the operation regions of accumulation, depletion, inversion and deep inversion. The student then compares 1D cross-sections of the carrier distributions at the center of the device with the predictions of the 1D "constant depletion width" approximation. With this comparison the student is able to analyze the validity and limitations of the "constant depletion width" approximation.

Lab 5: The student extracts "MOS Level 1" compact model parameters from TCAD device simulations for a 5-micron device as well as for a modern 0.13-micron device. Comparing these two devices the student is able to observe that the "MOS Level 1" compact model is well suited for a long-channel device, but is completely inadequate for the modern short-channel transistor.

Lab 6: The student explores the "short-channel" and "reverse-short-channel" effects. The student simulates the threshold voltage roll-off curves of two nearly identical transistors. One transistor shows the regular short-channel effect, i.e., the threshold voltage decreases with the reduction of the gate length. The other transistor exhibits reverse-short-channel effects, i.e., the threshold voltage first increases before it decreases as function of decreasing gate length. Using the visualization tool TECPLOT, the student compares the 2D doping profiles of the two transistors and can observe a link between the inhomogeneous channel doping (Halo) and the reverse-short effect.

Availability of TCAD simulation tools

A commercial single user TCAD license typically costs between several $10,000 and $100,000. However, some vendors have special programs for universities. The University of the Pacific acquired a full-featured teaching package with multiple licenses from ISE [1] for a nominal one-time fee. ISE designed this package especially for use in the classroom and student labs. The teaching license restricts complexity (node count) of structures. The node count, however, is large enough to perform 2D simulations of most device structures covered in undergraduate courses. (A research package with 3 user licenses and no node-count restrictions is also available for universities.)

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Julie Kenrow

Dr. Kenrow is an assistant professor in the Electrical and Computer Engineering Department at the University of the Pacific since 1999. She was a post-doc in the Physics Department at the University of Florida for 3 years and obtained her Ph.D. in Electrical Engineering from the University of California, Berkeley in 1994.