Dr. Hasina F. Huq is an assistant professor at the University of Texas-Pan American, TX, U.S.A. Her research interests include electronics device characterization, VLSI system design, and wide bandgap (WBG) semiconductor. She received her M.S. in Electrical and Computer Engineering from Virginia Polytechnic Institute and State University, Blacksburg, in 2002 and Ph.D in Electrical and Computer Engineering from the University of Tennessee, Knoxville, in 2006.

Dr. Huq has more than twenty papers published in peer reviewed international/national conferences and journals. She is a member of IEEE, IEEE Education Society and IEEE Power & Energy Society. Currently, Dr. Huq teaches Electronics, VLSI System Design, Advanced Solid State Device courses.
Integration of Nano Scale Electronics Devices into Undergraduate Course Curricula

Abstract

As deep-sub-micron and beyond technology emerges; integration of nano scale devices into undergraduate curricula becomes more important than ever. This paper addresses issues related to increasing impact of the nano electronics on undergraduate education in electrical and computer engineering courses. The purpose of the research is to present the class behavior, lessons learned, possible challenges and recommendations that may be used to promote simulation based learning and also the use of nano scale devices in electrical and computer engineering courses. The integration of simulation based learning (using simulation tools available at nanoHUB.org) helps the students to understand the nano devices concept. There is a strong need for well-educated nano electronics device design engineers and therefore, undergraduate-level training efforts are essential to meet future challenges related to nanotechnology. So the paper proposes a suitable educational topic for undergraduate VLSI course in electrical and computer engineering program. The assessment results not only show that learning indeed occurs during lab sessions, but almost equally as much (45%) as in lectures (55%). Also, it is observed that even students, who have no prior experience in nano scale devices, benefit from the simulation tools available in nanoHUB.org and incorporate the concept of nano scale devices in VLSI curriculum.

Each student team develops a nanoscale MOSFET structure and simulates them for their I-V characteristics. The critical parameters are doping concentration, materials properties, oxide thickness and aspect ratios (W/L). Then they have compared and analyzed their results with micro level devices. Thus, the students not only understand design issues at the nano scale level, but also experience the impact of design decisions at the device levels. Introduction of nano devices in VLSI curricula also help the students learn nano technology.

Introduction

The paper describes our experience in teaching nano scale devices in an undergraduate course, which convinced us that it is possible to integrate nano scale devices in VLSI course through design projects. As the deep sub micron and beyond technology emerges, training efforts in nano scale device characterization becomes more important than ever [1-5]. The research is motivated by the significant increase of education and training ability in nano electronics areas at undergraduate level. It is estimated that about two million nanotechnology workers will be needed worldwide in the field of nanotechnology by 2015. One of the grand challenges for the future development and implementation of nanotechnology is the education and training of new generation engineers. The performance of the nanoscale device simulation is carried out using nanoHUB.org. The purpose of the research is to present the class behavior, lessons learned, possible challenges and recommendations that may be used to promote nano technology based learning. Thus, students not only understand design issues at the nano levels, but also experience the impact of design decisions at the device level. It is also important to determine if such simulation based learning is still effective for student learning [7, 8, 9].

Methodology
The performance of the nano scale device simulation is carried out using the website www.nanoHUB.org. Each student has created an account to carry out the simulation. The specific simulation tools are then launched. The simulation tools allow users to enter their own data and parameters to perform a specific task. Users can access these tools and perform simulations remotely through the website. This web based simulation makes it possible to provide a simulation based laboratory experience to many off-site users. The following simulation tools are used to promote nanotechnology education through simulation-based learning.

- MOSFet & nanoFET: 2D simulator for thin body MOSFETs, with transport models.
- FETToy: Simulates I-V characteristics of conventional MOSFETs, Nanowire MOSFETs and Carbon NanoTube MOSFETs.
- CNTbands 2.0: Simulate electronic band structure and density-of-states for carbon nanotubes (CNTs).

MOSFet tool is used to observe the short and long channel effect. The FETToy tool simulates different types of MOSFETs from the regular metal oxide semiconductor transistors to the nanowire MOSFETs to the carbon nanotube FETs and provides their I-V characteristics. CNT Bands v2.0 provides a clear understanding of the effects of the chirality vectors in real space \( n \) and \( m \), and how its coefficients create a semiconductor or a conductor. The critical parameters are doping concentration, materials properties, oxide thickness, gate electrode, temperature, and different aspect ratios \( W/L \). The introductory VLSI course covers the principles of device design and operation: logic gates that define system performance, end-system applications. To address the challenges and major limitations, simulation based nano electronics learning module have been proposed at no cost.

Text Book, References and prerequisite: The following books and references are used for the course:

- Ken Martin, Digital Integrated Circuits design, Oxford
- H.Craig Casey, Jr., Devices for Integrated Circuits, John-Wiley, Baker, Li, & Boyce,
- Cadence manual set & Simulation tools & lecture notes @ nanoHUB.org
- Class handouts

The prerequisites are ELEE/CMPE 2330: Digital Systems I and ELEE 3301: Electronics I (junior standing as prerequisites) or equivalent courses with a grade of ‘C’ or better. Students are expected to be familiar with digital logic gates; and MOSFET properties.

Project Description: Each student team develops nano scale MOSFET and CNT based FET structure and simulates them for their I-V characteristics. Then they have compared and analyzed their results with micro level devices. During weekly meetings the student group presents their simulation results to the instructor for review. Based on the instructor’s feedback and group discussion possible improvements are made.

Sample #1

Objective: The part of the project involves nano scale MOSFET characterization. The main objective of the lab is to expose the feature of nano devices that are important for a good learning experience for the students who have no prior experience in nano technology. The
lab has been designed to hide the complexities of configuring high-performance nano scale devices.

Figure 1. Example of problem using MOSfet tool:

Task assigned:
I. Design (Construct) MOSFETs and compare the behavior as a function of various parameters.
   A. Examine the effect of doping on $V_T$.
   B. Examine the effect of metal electrode material on $V_T$.
   C. Examine the effect of oxide thickness on $V_T$.
II. Design (Construct) long- and short-channel MOSFETs and Identify the performance limit.
   A. Examine the effect of SOI material on $V_T$ (for short channel)
   B. Demonstrate the effect of channel length on the electric field.
   C. Examine the effect of channel length on $I_D-V_D$
III. Repeat II for nanoFET and FetToy tool

Discussion: The students are able to compare the threshold voltages of MOSFET devices at nano level. Students have also demonstrated the stable operation of the nano FET devices at room temperature. The students are also asked to analyze the output and input characteristics (Id-Vd, Id-Vg) of FET over a temperature range to examine the temperature effects. Then the students identify the doping effect at various temperate with minimum channel length. The projects also involve the effect of gate electrode (N+poly, P+poly, Al, Tungsten) with minimum doping and channel length. Aluminum as gate electrode contributes more currents compare to other electrode. The students have observed the I-V characteristics with different processes which involves PMOS, NMOS, NSOI, PSOI processes. As the temperature increases the maximum current drops due to the effect of mobility. Students have also demonstrated that the higher doping level is better for stable operation of the nano FET devices. Finally they are able to see the total scaling effects at micro and nano level.
Sample #2

Objective: In this problem, the students are able to compare the effect of aspect ratio of micro and nano scale FET devices at room temperature. They use the transistor equivalency concept to replace the driver network.

Example: 
\[ f = \overline{(A \cdot B)} + C \]

![Transistor equivalency concept diagram](image)

Figure 2. Example of transistor equivalency concept

Task: In this problem, students are given a function. From the given function they have generated the transistor level schematic. The W/L ratios are given. Then the students are asked to replace the drive transistor network by a single equivalent transistor and to find the W/L ratio of the single transistor using conventional MOSFET and nano scale MOSFET.

Discussion: After investigating all of these properties the students have finally established the phenomena that the nano FET devices can give us faster speed, smaller and thinner system solution with low power loss. But the main difficulty is the fabrication facilities.

Sample #3

Objective: In this lab, the students investigate the electronics property of Carbon Nano Tube (CNT) and their application in nano electronics. CNT can be metallic or semiconducting based on the direction of graphene sheet roll. Understanding in detail the nature of the direction of graphene sheet roll is therefore an important ingredient in the study.

Task: The students use the simulation tool CNTbands2.0 to simulate Density of State (DOS) and energy gap of CNT. The tool helps to simulate different types of CNT. The (13, 0) nanotube acts as semi conducting material since it has energy gap between conduction and valence band. The (10, 10) nanotube and the (10, 5) nanotube act as conducting material as the valence and conduction bands overlapped.
Discussion: The band gaps of CNTs are small (from 0.2 to 2.0 eV). So CNTs are either metallic or semiconductive. The energy band structures of carbon atom C provides an occupied energy level in the band gap depending upon the DOS and types of CNT. CNT based transistors are expected to use in high performance electronic devices such as in memory circuits or RF switches, optoelectronic devices, biomedical instruments, nano-electro-mechanical-systems (NEMS), as well as in other areas of application.

Assessment Methodology

In this study, student learning is assessed throughout a course CMPE/ELLE 4375 “Introduction to VLSI”. This course is taught by the author in fall 2009 at the University of Texas-Pan American. ELEE/CMPE 4375 is an undergraduate course that is required for the computer engineering program and is also often taken by Electrical Engineering students as an elective course. Some of the lectures topics are also suitable for Master’s students. Thus, students have a broad range of background knowledge ranging from no prior exposure to nano electronics to being researchers in the nano technology. The course consists of 20 lectures, four homework assignments, one midterm and seven lab assignments. All lab topics are covered to some extent in lectures. The lab assignment topics and related VLSI concepts covered in the courses are shown in Table 1. The following question is addressed in the assessment study; do the students benefit from use of nano electronics concept. An assessment methodology is developed that distinguishes between learning in lectures and learning in the labs. Thus, it is assumed that lectures precede lab exercises. In such a scenario, students may learn during the lecture and/or may learn during the lab. The authors have used the following assessment methods as proof that students have learned during the class: quiz, test, research paper, homework, one-on-one conversation, project, final exam. Formative assessment (quiz, research paper, homework, one-on-one conversation) informs students how well they have learned and also informs the instructors how well the learning activities are helping students.
Summative assessment (test, final exam) measures the overall students learning. The following assessment steps are used during the semester. First assessment: pre-lecture assessment of prior knowledge. Second assessment: post-lecture and pre-lab assessment of learning during lecture. Third assessment: post-lab assessment of learning during class. Students did not know what questions they would be asked. For each lab topic, the authors have created a set of open ended questions that covers the most important concepts. Sample examples of such questions are shown in Figures 1, 2 and 3. If a student does not answer a question correctly in the first assessment but then answers it correctly in the later assessment, it is inferred that learning took place during activities related to the lecture. Of course, there are numerous sequences of events that can take place [13-16].

Table 1. Laboratory Assignments

<table>
<thead>
<tr>
<th>Lab</th>
<th>Concept</th>
<th>Lab Assignments</th>
<th>Amount of Lecture</th>
<th>Amount of using Cadence</th>
<th>Amount of using Nano HUB</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Logic gates</td>
<td>Standard cell design, Device characteristics</td>
<td>30%</td>
<td>60%</td>
<td>10%</td>
</tr>
<tr>
<td>2</td>
<td>Digital system design</td>
<td>Flip flop design, Adder design</td>
<td>20%</td>
<td>80%</td>
<td>NA</td>
</tr>
<tr>
<td>3</td>
<td>Analog system design</td>
<td>Mixer, Amplifier, Current mirror</td>
<td>30%</td>
<td>70%</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Nano scale devices</td>
<td>MOSFET, FETtoy, CNT FET</td>
<td>55%</td>
<td>0%</td>
<td>45%</td>
</tr>
</tbody>
</table>

Results

The results of the presented study are based on data collected during one semester. A total of 30 students have participated in the study. Each student has provided informed consent to collecting this data. Also, some data is anonymized and is presented in aggregate form to avoid exposure of any personally identifiable information. The nano electronics lecture module has given a good introduction to the various phases involving the design of an integrated circuit at nano scale. The modules can be directed towards the goal of establishing first-rate nano technology research and educational programs at most of the US institutions. The students have demonstrated that the challenges of FET design at nano level enhanced their device design skills. Students can be involved in research and can spend more time to produce substantially better design solutions in terms of size, cost, and power consumption. A study involving more complex design with nano electronics may produce observable differences in design quality. Formative and summative process data is utilized to provide feedback.

Conclusion

It is observed that even students, who have no prior experience in nano scale devices, benefit from the integration of nano scale devices in VLSI course curriculum. The developed modules also help to educate and train engineers in nano-electronics with a focus on FET.
based device characterization. Nano electronics allow fabrication of much smaller transistors with superior electrical properties. So significant system benefits are anticipated from nano electronics devices; however, there are many technological and material challenges for them [9, 10]. The lecture module has served as a channel to connect the students with the latest technology and it also allows them to be aware of their own ability in technology innovation. Understanding the nano electronics concepts will inspire students’ interests in multiple science and engineering disciplines, and prepare students for the interdisciplinary nature of future technology.

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References

Biographical Information

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