



## Introducing Nanotechnology into an Undergraduate Microelectronics Course

### **Prof. Chung Hoon Lee, Marquette University**

Chung Hoon Lee is an Assistant Professor in the Department of Electrical and Computer Engineering at Marquette University, Milwaukee, WI.

### **Dr. Susan C. Schneider, Marquette University**

Susan Schneider is an Associate Professor in the Department of Electrical and Computer Engineering at Marquette University, Milwaukee, WI. She is also the Director of Undergraduate Laboratories for the Electrical Engineering program. Dr. Schneider is a member of ASEE, the IEEE, Sigma Xi and Eta Kappa Nu.

### **Mr. Trevor Thiess, Marquette University**

# Undergraduate Introduction to Micro-fabrication of Memristors

## Abstract

In Spring 2012, a pilot project to increase student exposure to nanotechnology was carried out in the first electronic devices course in the electrical engineering program at our university. Students were given the opportunity to build and test memristors in the nano-electronics research laboratory under the supervision of their instructor. In this pilot project, 10% of the students in the class chose to participate. Based on the success of the first trial, this project will be run again in Fall 2014.

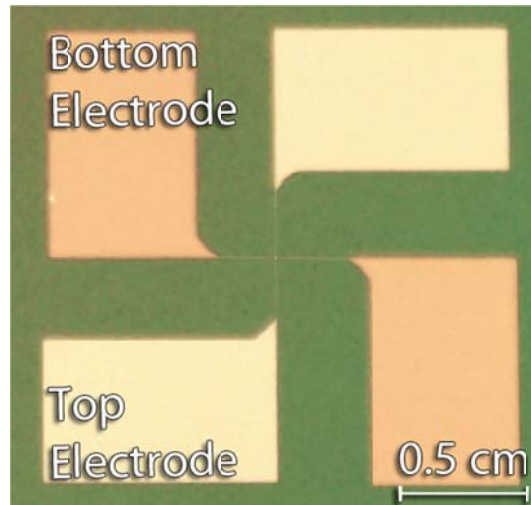
The topic of “memristors” was chosen for this project motivated in no small part by the fact that these devices are currently “hot” in the microelectronics/nanoelectronics research community. An additional attribute, deemed essential for this student experience, is the ability to create a macro-scale version of the memristor. The project work included mini-lectures and assigned readings on the history, theory of operation and fabrication, and applications of these devices. The project consisted of two sections: macro-scale and micro-scale memristors. During the macro-scale portion of the project, students practiced the memristor fabrication techniques for several different base metals and sulfiding mediums. Then based on the results (either success or failure) determined by the measured current-voltage characteristics of the memristor, the students made choices on the materials and methods to scale down the macro-scale memristor to the micro/nano-scale memristors using an industry standard fabrication techniques. A graduate student working in the nano-electronics laboratory assisted the students during all experimental work including safety training and help on both fabrication and data acquisition.

## 1. Introduction

A memristor is a passive electrical circuit component proposed to explain non-linear circuitry by Leon Chua in 1971 [1]. In 2008, an HP Labs team realized the conceptual fourth component in circuit theory [2] by fabricating a  $\text{TiO}_2$  based memristor. A memristor is characterized by its ability to ‘remember’ previous resistance states. A memristor is a non-volatile device able to maintain its state when it experiences either no voltage or constant voltage (device off or steady-state). It relates electrical flux and charge as a resistor relates electrical current and voltage [2].

A team of second year undergraduates was assembled to pursue research into memristor design, fabrication, measurement, and analysis. A prototype of the memristor students fabricated is shown in Figure 1. The students were recruited during an introductory lecture on solid-state principles in their microelectronics course by introducing the burgeoning field of memristor research and commercialization. The class was shown a video on the memristor and its potential in the future of electronics was discussed. The basics of the memristor were explained alongside the diode; each placed within its own historical context—both symbolic of transitions in the way engineers imagine circuitry.

A conversation progressed over a few weeks of lecture and eventually led to a team of seven students being formed to investigate memristor fabrication. The team included biomedical,



*Figure 1. A micro-scale memristor fabricated by second-year undergraduate student teams.*

electrical, and computer engineers. Arrangements were made for short after-class meetings and three focused lectures on the memristor.

## **2. Mini-Lectures**

Three lectures served to bring all students up to speed on the material as well as establish a common understanding amongst them. This facilitated team communication and coordination early on in the project.

The first lecture covered the history of the memristor. The discussion focused on the progression of the memristor from theory to the prototype developed 37 years later. Students learned that the device had been proposed by arguing that inherent circuit element symmetry pointed to a theoretical device relating electrical flux and charge [1,2]. Discussion was focused on how to use the theoretical guidelines to design a development plan for their memristor.

The second lecture focused on the memristor's principle of operation and the characteristics of I-V curves. The switching mechanism of the memristor was explained by the I-V curves. Using the course material as reference, students learned how the seemingly subtle differences between the devices from their course lead to dramatic electronic differences in the memristor. The second lecture consisted of how the fabrication techniques gave rise to such principles – such as the electron tunneling phenomena and how the reduction of a metal forms a charge boundary within the device capable of controlling the electron dynamics through the two terminals. The students were asked to carry on their own research on the applications of their field in preparation for the next and final lecture.

In the final meeting, student compared notes and assembled a more comprehensive list of the techniques employed in previous research efforts. Unfamiliar techniques were explained, such as evaporation deposition and sputtering. Students learned which tools would be available in the lab and devised a plan that utilized materials and tools to carry out their own memristor fabrication.

### 3. Preliminary hands-on experiments on a macro-scale memristor

To explore and choose the appropriate metals and the metal reduction (sulfiding) methods, a macro-scale prototype was fabricated. Three metals and three sulfiding methods were used to find an optimal material and method for micro-scale memristor fabrication. The chemical reduction of metals with sulfur was also demonstrated by three techniques: direct sulfur powder contact, sulfur vapor produced by heating sulfur in furnace, and wet chemical sulfur solution bath. Table 1 summarizes the metals and sulfiding methods and results.

The powder reduction method is done by exposing bulk metal directly to sulfur powder in a container. The reaction between the copper and sulfur occurs at a slow rate at room temperature, which allows students to execute the experiment in a 24-hour trial. After reduction, the surface of the metal appears charcoal-like, matching the appearance of copper and silver sulfide. In the case of aluminum, no color change is found, indicating no or an extremely slow reaction. Aluminum shows poor reaction for the other sulfiding methods as well. Due to the poor reaction between aluminum and sulfur, an aluminum block has been chosen to be an electrode material for the memristor.

*Table 1. Results of macro-scale metal sulfiding methods.*

	powder	furnace	wet chemical
copper	fair	good	fair
silver	fair	fair	good
aluminum	poor	poor	poor

Although the powder sulfiding method was simple and repeatable for producing metal sulfides, the method produced non-uniform sulfide films across the metal surfaces. To improve the uniformity of the sulfide film, chemical vapor method in a quartz furnace was used (indicated as furnace method in Tables 1 and 2). To produce the sulfur vapor, sulfur powder was heated in a quartz tube furnace (the detailed procedure is given in the following section). While sulfur was heated, metals were placed near the sulfur source. By visual inspection the surface of the metals appeared to show the same type of reaction, but with better film uniformity than the powder method.

The two sulfiding methods (powder and vapor) were compatible with the micro-scale memristor fabrication. The limitation of these two methods was the sample size. In the case of micro-scale fabrication, a 4-inch diameter wafer would be the standard size. The powder and vapor methods were impractical for the 4-inch diameter wafer scale. Another reduction method explored was the wet chemical bath procedure. This method involved exposure of a bulk material to a solution of sulfur compounds (called “Liver of Sulfur”). After exposure to the bath for a designated length of time, the prototype was left to dry. This method also produced charcoal-like film for copper and silver.

To confirm the sulfided film was the proper material for a memristor, the I-V curve was measured. In order to make the I-V measurement, two electrodes were connected to the bulk sample. By scratching a corner of the sulfided surface, the host metal was exposed and used as

one electrode. A 20-gauge aluminum wire was used for the other electrode. The electrical contact of the aluminum wire to the sulfided film was made by a gentle mechanical touch of the wire to the film. The measured I-V characteristics of the reduced film showed the characteristics of a memristor reported in the literature and a computer simulation of the theoretical memristor I-V curve.

Macro-fabrication served as an important guide for students to carry on the micro-scale experimental method. The macro-scale fabrication methods showed various sulfiding methods, which could be used in the micro-scale memristor fabrication. Students also completed the I-V measurement setup to measure the I-V characteristics of a memristor.

#### 4. Fabrication of a micro/nano-scale memristor

With the successful fabrication and demonstration of macro-scale memristor, students proceeded to the micro/nano-scale memristor fabrication and I-V curve measurements.

##### 4.1. Design

The complete design crosses two pairs of electrodes at a  $90^\circ$  angle as shown in Figure 2, creating one junction (the device itself), where one overlaps the other. The four-electrode configuration allows the device to be measured in four different possible orientations by choosing neighboring electrodes in clock-wise rotation. The electrodes are made from either silver [4] or copper and are created by metal deposition in a thermal evaporator [3]. The memristor layer is created on the surface of the bottom electrode by reduction developed in the macro-scale fabrication. After the memristor layer is in place, the top electrode is deposited over it in the same way as the bottom electrode with  $90^\circ$  degree rotation of the shadow mask. The target size for the memristor was about 5 by 5 microns square.

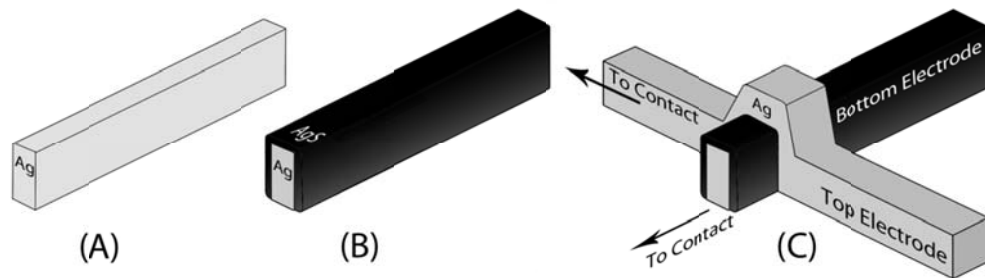


Figure 2. Design of micro-scale memristor and process flow. (a) silver metal wire (b) sulfiding Ag. (c) deposit top-electrode in  $90^\circ$  degree rotation.

##### 4.2. Memristor Fabrication

As shown in the Figure 2, the first step of the micro-memristor fabrication process was to define a single micro/nano-scale metal wire on a substrate. A thermally oxidized silicon wafer or microscope cover glass could be used as a substrate for the memristor fabrication. In this project, a 4-inch silicon dioxide film ( $\text{SiO}_2$ ) coated silicon wafer was used. On each wafer, twelve devices were accommodated.

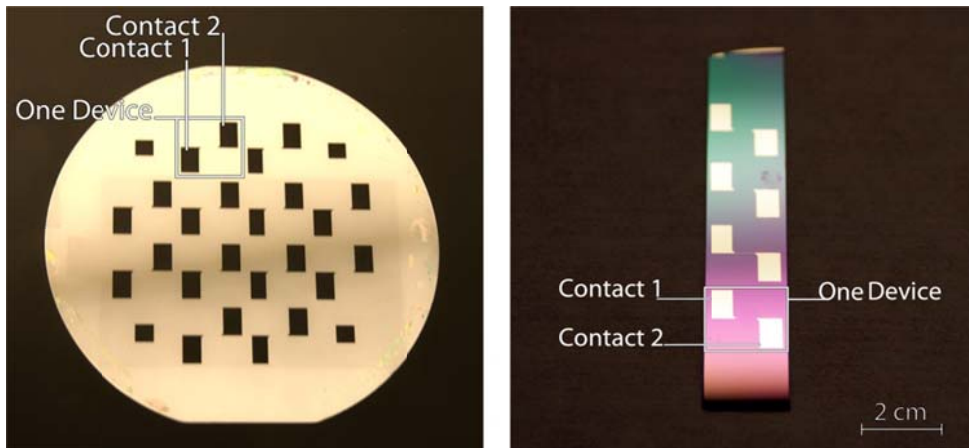


Figure 3. (a) shadow mask (b) patterned metal wire with contact electrodes by the shadow mask process.

Defining the metal wire at micro/nano-scale is typically done by optical lithography to transfer the design to substrate and wet chemical etching to define the pattern of the wire. However, in this project, a shadow mask process to define the wire was chosen for the fabrication simplicity. A shadow mask for the metal wire patterning was provided to the students. The use of a shadow mask eliminates complications of optical lithography and chemical etching of metal layer, which were beyond the capability and time scale in this project for undergraduates. Another advantage of the shadow mask method was that once it had been created it could be reused to pattern the wire and electrodes (top & bottom) for each device fabrication.

The shadow mask used in this project was fabricated by a typical micromachining technique utilizing optical lithography, reactive ion etch (RIE), anisotropic wet chemical silicon etching. The shadow mask was then affixed to the silicon wafer (substrate) and placed in the thermal evaporator. After metal evaporation with desired thickness, the shadow mask was detached from the silicon wafer leaving the patterned metal wires on the substrate. The shadow mask and a slice of a wafer containing the patterned wires are shown in Figure 3.

#### 4.3. Sulfide methods

As briefly described in section 3, students developed three sulfiding methods. Although all three methods led to a successful metal sulfided film in macro-scale memristor fabrication, the furnace and wet chemical methods were used in micro-scale memristor fabrication. The powder method was eliminated because the method left many particles on the substrate which interfered with the following top-electrode deposition.

##### 4.3.1. Furnace Method

The sulfur vapor method uses a quartz tube furnace to accelerate sulfur sublimation as shown in Figure 4. The furnace temperature, 200 °C, is set higher than the melting point of sulfur, 115 °C. An alumina boat of sulfur is placed in the center of

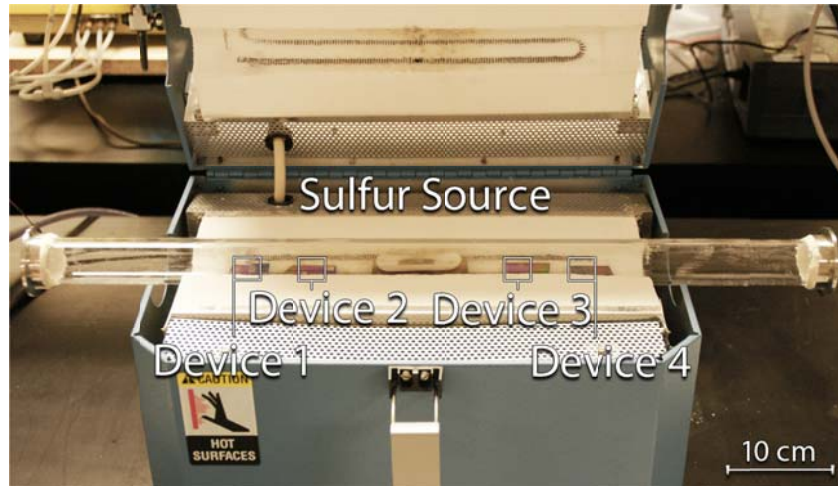


Figure 4. Quartz tube furnace for sulfur vapor sulfiding method

the furnace's quartz tube and devices are positioned in multiple places to study the temperature effect of the sulfiding. The positioning of devices with respect to the sulfur source and the temperature is varied across the trials. Devices are placed directly adjacent to the sulfur source (2 & 3 in Figure 4) and above the boundary of the furnace's insulation (1 & 4 in Figure 4). A record of trial runs is summarized in Table 2.

The sulfur vapor method produced a wide variety of conditions, but also yielded the most functional devices. This indicated that the method needed much more careful tuning before it could be a reliable process, but that it did have great potential for this use. A major drawback to this method was that it was an individual-device process.

#### 4.3.2. Chemical Bath

Chemical reduction via sulfur solution was favored for its simplicity and most importantly, its ability to be scaled up to full-wafer production. The device was submerged in a solution containing sulfur ions for a specific duration. The surface of the metal reacted with the sulfur ions creating sulfided surface.

The chemical bath method was a more easily controlled process with fewer variables than the furnace method. However this method produced no devices that displayed memristive behavior in this study. Microscopic investigation showed that the intended reaction seemed to occur as judged by the color and granularity of the metal surface after sulfiding. It turned out to be that the absence of memristive behavior was due to the initial thin metal layer. The thin metal layer was entirely sulfided. Several attempts with various concentrations and reaction times were not successful to produce devices showing the memristive behavior. Further investigation on the chemical compositions of the "Liver of Sulfur" and concentration might produce the memristive film as the macro-scale case in the section 3. The sulfiding parameters used in chemical bath method are listed in Table 2.

Table 2. List of each sulfiding condition parameters for both Ag and Cu for both the furnace and chemical bath method.

Metal	Adhesion Layer	Bottom Electrode	Reduction	Time	Temperature (°C)	Top Electrode
Ag	N/A	100 nm	Direct Contact (no heat)	24 hours	20	450 nm Ag
Ag	N/A	100 nm	Furnace (on boundary)	18 minutes	120	450 nm Ag
Ag	N/A	100 nm	Furnace (on heater)	10 minutes	200	450 nm Ag
Ag	N/A	100 nm	Chemical Bath	30 seconds	20	450 nm Ag
Ag	130 nm Ni	400 nm	Furnace	10 minutes	200	450 nm Ag
Ag	130 nm Ni	400 nm	Chemical Bath	30 seconds	20	450 nm Ag
Cu	N/A	500 nm	Furnace (on boundary)	10 minutes	200	300 nm Al
Cu	N/A	500 nm	Furnace (on heater)	10 minutes	200	300 nm Al
Cu	N/A	500 nm	Furnace (at end of tube)	10 minutes	200	300 nm Al
Cu	N/A	500 nm	Chemical Bath	30 seconds	20	300 nm Al

#### 4.4. Top Electrode Deposition

Once the metal sulfided layer was created, the devices were mounted to the shadow mask with 90° rotation with respect to the initial pattern of the metal layer. Then the second metal deposition to create the top-electrode was done in the thermal evaporator. The second evaporation of top-electrode completed the memristor fabrication. A close-up optical image of the device after the second metal evaporation is shown in Figure 5. To determine the quality of the junction created between the overlapping micro-wires, the electrical resistance between the electrodes was measured. Typical resistance for the junction was about 3.5 kΩ. Among the 12 devices, 10 devices showed the typical junction resistance values and the other two devices were electrically shorted.

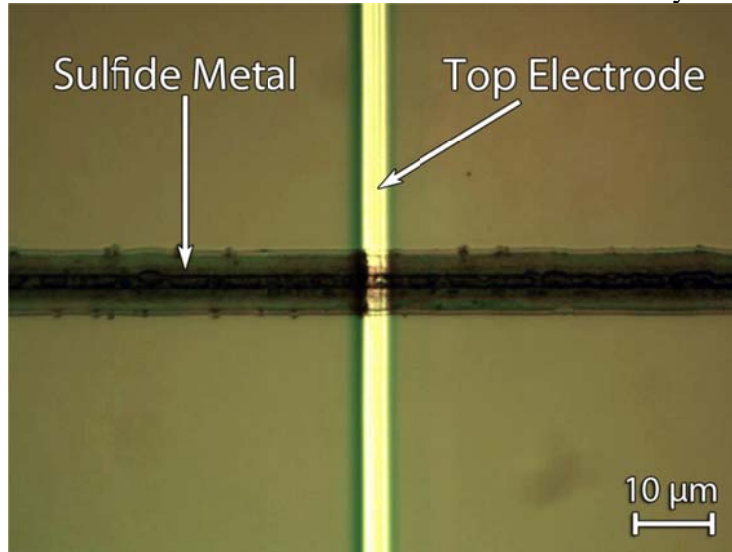


Figure 5. A close-up image of the junction, metal-metal sulfide-metal.

### 5. I-V Characteristics of the micro-scale memristor

Prototypes were prepared on an insulating acrylic plate. Thin electrical wires (24-gauge) were taped to the electrode contacts and the other end of the wires was clamped on the side of the acrylic plate as shown in Figure 6. Typically, the terminal contacts were created using a wire-bonding method, but here a mechanical contact with a Kapton tape simplified the procedure. The



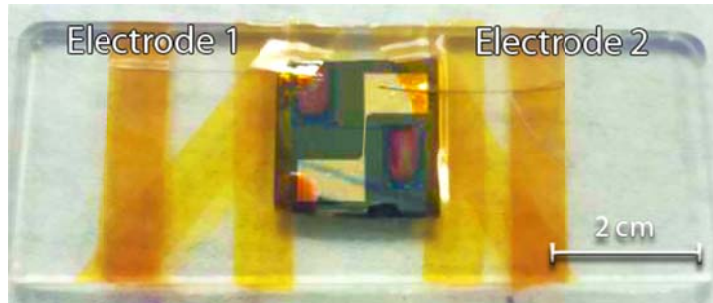


Figure 6. Preparation of device for I-V characteristic measurement.

wire-bonding was avoided because of further process complications such as optical lithography and Au evaporation for the contact pads.

The I-V characteristic measurement setup is shown in Figure 7. The computer communicates with the function generator via GPIB. A custom Labview program controls the function generator. The function generator is set to output AC voltage (sine wave) on one of the memristor electrodes. The AC voltage is also fed to channel 1 on the oscilloscope, which represents the x-axis (applied voltage). To represent the typical memristor I-V characteristics, the output current is converted to a voltage and plotted with the input voltage. To do this, the second electrode is connected to a resistor (1 k $\Omega$ ). A probe is connected between the second electrode and is fed to channel 2 of the oscilloscope, representing the y-axis.

With the setup, a typical I-V characteristic curve of the micro-scale memristor is shown in Figure 8. All working devices show similar trend of the curves. The device shown in the Figure 9 (a) is a copper device reduced by the furnace method for ten minutes at 200  $^{\circ}\text{C}$ . Figure 9 (b) is the I-V characteristic curve of the memristor simulated by a PSPICE model. The asymmetric behavior of the I-V curve is due to the different metal electrodes on the memristor. If the electrode material is the same metal and the junction condition between the metal and sulfided metal is identical on the both electrodes, the I-V curve will be symmetrical.

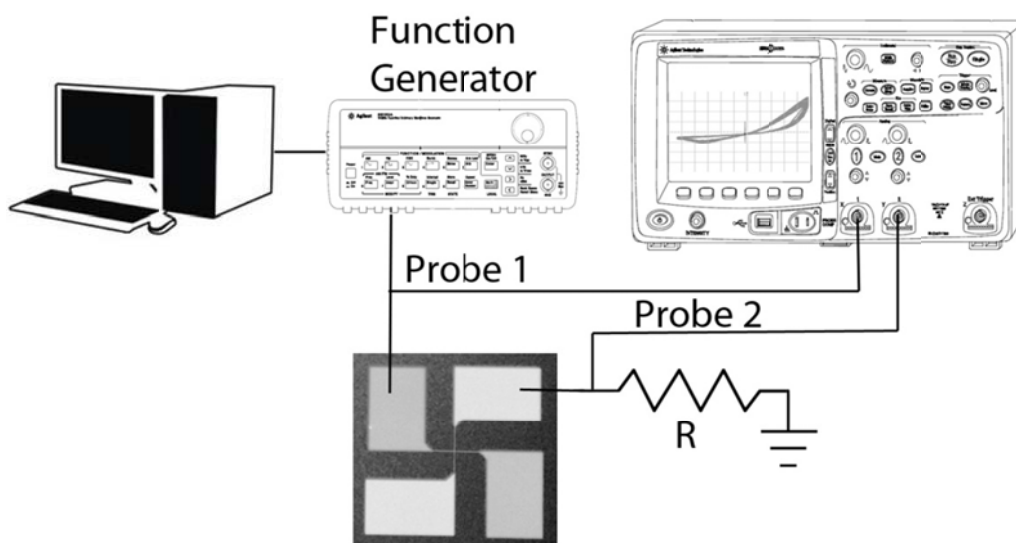
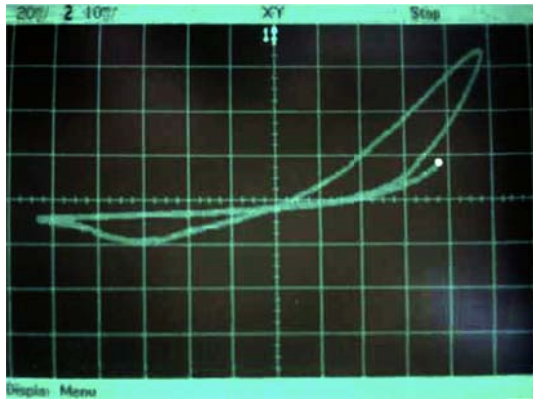
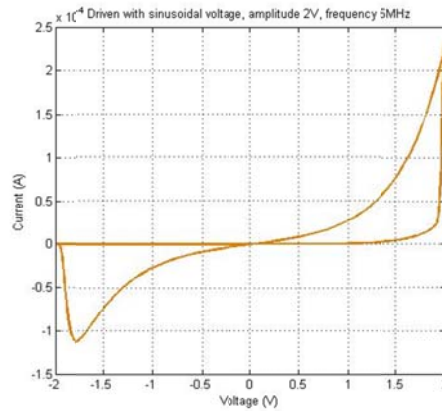


Figure 7. Memristor I-V measurement setup



(a)



(b)

Figure 8. I-V characteristics of a memristor (a)measured I-V curve of the micro-scale memristor. (b)simulated I-V curve of the memristor by PSPICE.

## 6. Discussion

The most promising results came from the copper samples. This is possibly because the silver prototypes were made with a relatively thinner initial deposition, leaving them too prone to the entire material being reduced without leaving electrode metal. Memristor I-V characteristic curves were observed on almost all devices (90 %) from different methods, although the copper devices demonstrated the most stability and repeatability.

The chemical bath method needs further refining in order to be a viable means of production. Possibly the solution needs to be more finely controlled to ensure that only the intended reaction is occurring. In these trials a Liver of Sulfur solution was implemented, which contains a variety of sulfur compounds and could lead to different sulfides developing. In the future more variables could be added to the technique such as heating the solution before reaction.

Figure 9 shows the variety of results observed over several reduction methods. Devices 4 & 5 demonstrate the difference in placement within the quartz furnace tube; although device 4 was positioned the farthest from the heater, it demonstrated a more deep reduction than device 5. Both devices 4 & 5 appeared to need further exposure time to complete reduction. Device 9, reduced in the same trial, exhibited what appeared to be heat damage. These three devices (4, 5, & 9) indicate that less heat and more time in the furnace could lead to a more effective reduction of the metals. Similar reduction occurred in the silver furnace trials (as shown by device 6). The Chemical Bath method yielded a more complete and uniform reduction of the surface metal, as shown in devices 2 & 3.

A common trend appeared during the measuring of untouched prototypes. They would have a similar 'sweet spot' for functionality, mostly proportional to their initially measured resistance, but after a few minutes of expected behavior, the area within the looped I-V curve would collapse and become a flat resistance, indicating an open circuit. After disconnecting the device from the measurement setup for a few minutes, the device shows the characteristic I-V curve

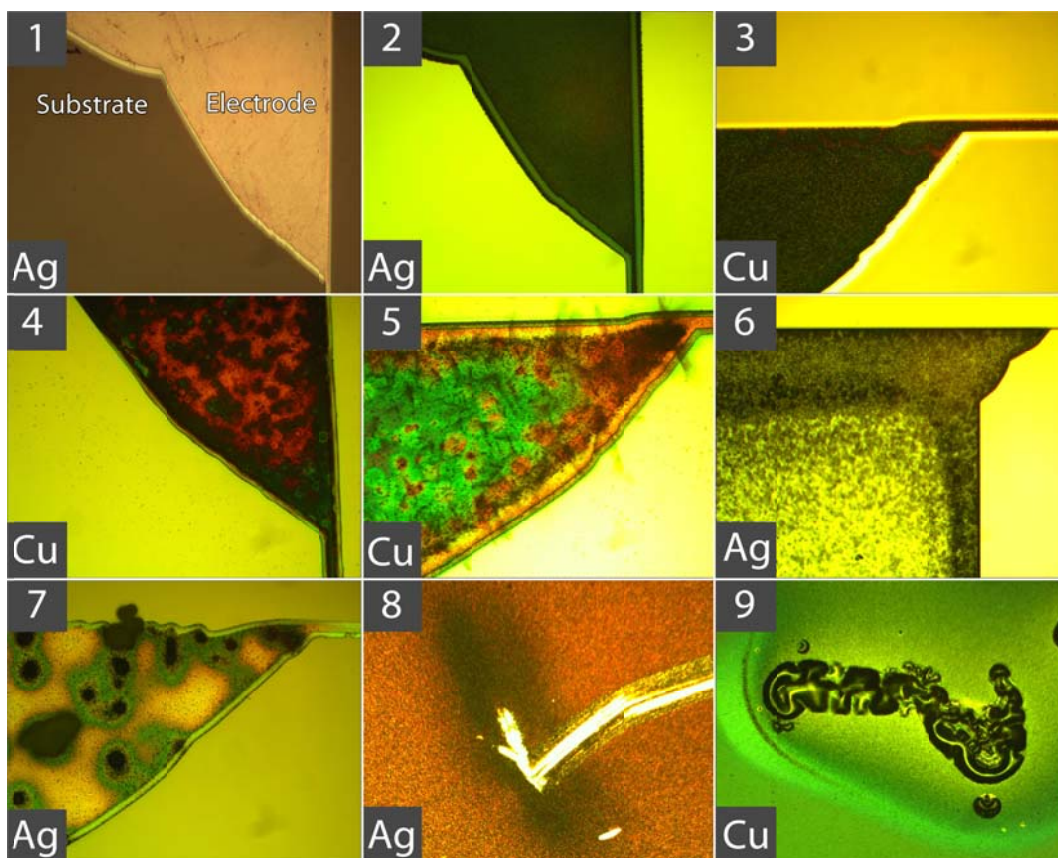


Figure 9: Physical Results of Reduction by Various Methods.

- 1: Electrode before reduction
- 2: Same electrode as in 1, post-reduction (30 second Chemical Bath)
- 3: Exposed to sulfur solution (chemical bath) for 20 seconds
- 4: Exposed to sulfur vapor at 200 °C for 10 minutes (placed at end of quartz tube)
- 5: Same trial as 4, but placed in between the center and the end (boundary)
- 6: Exposed to sulfur vapor at 200 °C for 10 minutes on boundary
- 7: Reduced by direct exposure to sulfur powder
- 8: Probe damage observed on 100 nm Ag post-reduction (15 second chemical bath)
- 9: Deformations in copper observed when placed directly on heater (10 minutes)

again when connected to the measurement setup. This phenomenon is probably due to the temperature increase due to the Joule heating at the junction interfering with the ion transport. Further annealing steps after device is fabricated may stabilize the temperature effect of the ion transport.

The research has demonstrated an effective fabrication technique for micro-scale memristors and cleared the path for high-potential advancements to the procedure by uncovering areas for improvement. Fabrication techniques can be further refined to address electrode adhesion issues, the failure of chemical bath process, the possibility of using annealing process, and poor

response in silver-based devices. Analysis techniques can be improved by further developing the probing method, controlling for “burning” out devices during measurements, and design of a measurement jig to ensure consistency.

The iterative approach implemented by the team was found to be especially useful for such a project because no one involved had a particularly deep understanding of the process initially; it allowed students to learn and explore a wider range of possibilities and see a broader spectrum of results.

The project proved to be very low-cost as well. The price was kept down by using many tools already found in typical electronics labs. The most significant costs were the shadow masks and the silicon wafers. A breakdown of necessary fabrication supplies is listed in Tables 3 & 4.

*Table 3: List of materials used with suggested alternatives.*

Material	Quantity	Description	Source	Suggested Alternatives
Substrate	1	4-inch Si wafer	Commercial	cover glass
Shadow mask	1	4-inch chemically etched shadow mask	Micromachining	narrow slits
Copper	1 gram	Bulk copper	Chemical supply	copper powder
Silver	1 gram	Bulk silver	Chemical supply	silver powder
Aluminum	1 gram	Bulk aluminum	Chemical supply	
Sulfur	5 grams	Sulfur powder	Chemical supply	
Liver of Sulfur	10 ml	prepared Liver of Sulfur (1) : DI H <sub>2</sub> O (1000)	Chemical supply	
Ployimide tape	1 roll	For holding substrate in evaporator and attaching contact wires	General supply	Kapton tape
Contact wire	1 foot	32 gauge wire to be taped to contacts for reliable measurement	General supply	Any sort of probe, especially spring-loaded.
Resistors		For use in device test circuit		
Cables		To connect test circuit		

*Table 4: List of equipment used with suggested alternatives.*

Equipment	Description	Suggested Alternatives
Evaporator	Vacuum evaporator for use in deposition of metal	Sputterer
Furnace	Quartz tube furnace for the reduction of base metal with sulfur	Hot plate with Pyrex glasses
Function Generator	For use in device test circuit	n/a
Oscilloscope	For use in device test circuit	n/a
LabView-enabled Computer	(Optional) For data-acquisition and equipment control in device test circuit.	Measurements and adjustments can be done manually
Microscope	(Optional) For assessing and visualizing the device throughout fabrication	Magnifier or camera

## 7. Student Evaluation

Students found this project very engaging because the subject matter was not commonly covered otherwise in undergraduate studies. Students liked being able to put in sizeable periods of lab-time, get hands-on experience with new tools, and learn about micromachining techniques. Students found analyzing the samples after reduction and comparing them across different methods to be very educational because it allowed them to see the molecular changes of material phase in each method. It is unique in that students implement a full cycle of research and development.

Making the introductory lecture meetings light and discussion-based fosters a friendly environment, which is conducive to team building. The mini-lectures are also very important for bringing all students to the same level of understanding and creating a common language amongst them. The students who participated least in this project were more likely to feel that they lacked understanding in the material. The more well-versed students were eager to get the project going and eventually dominated the project. This led the less familiar students to feel less confident contributing to the project over time. This problem can also be helped by working in small groups, allowing each student to participate in a specific, focused way.

The group size (3 or 4 students in each group) had its advantages. This group size allowed each student to lessen the time dedication they had to commit, which often made things more manageable. Although it had time benefits, splitting the team into shifts also opened up the possibility of creating parallel understandings between groups of students (i.e. the students who spent more time in the lab had more feedback and had a different understanding of the project plans & details). If all students were in the lab at the same time though, it could crowd the focus of the team and lead to dispersion of responsibility, often leading to the most confident or knowledgeable students participating the most. Ultimately, the number of students depends on many facets of the project: the number & availability of machines/tools, the amount of lab space & graduate student aid, and the comfort of the team with each other & the subject matter.

This project was a voluntary supplement to the required microelectronics course. Similar numbers of participants and levels of participation are expected if offered in the future based on student input upon completion of the project. Although students were interested in the project, some students found the time commitment to be too demanding. If inserted into a standard undergraduate electronics laboratory course, it could be more manageable for students because they are already prepared to plan for that amount of time in lab.

This project could be easily inserted into a standard undergraduate electronics laboratory curriculum with some modifications. Table 5 lays out the hours of commitment necessary to complete the fabrication of multiple device samples. At our university, the analog electronics lab consists of 3 large projects, each spanning 5 weeks and consisting of a three-hour time commitment once a week. Following the guidelines of this structure, the first lab would cover the three mini-lectures introducing and discussing the device. The following three labs would cover the fabrication procedure and testing would be performed in the final lab. If time constraints posed a large problem, lectures could be broken down into smaller mini-lectures and made available electronically through our university course management system and lab time can be cut down by preparation by a laboratory T.A. When converted into a larger classroom setting, lab groups can be assigned different materials and encouraged to investigate modifications to the reduction parameters (e.g. time, temperature, dilution, etc.).

*Table 5: breakdown of approximate time commitment of each step in the fabrication process*

Introductory Lectures	First Evaporation	Furnace Reduction	Chemical Reduction	Second Evaporation	Testing
3 hours	1 hour	2 hours	2 hours	1 hour	2 hours

## 8. Conclusion

The two teams successfully developed a fabrication technique that produced functional memristors. Fabrication research concludes that reducing copper to copper sulfide to form the insulation layer of a memristor by means of a sulfur vapor method is an effective way to realize memristive behavior. The overall structure of the project was successful and valuable to students. This project demonstrates an effective path for introducing nano- and micro-electronics engineering to undergraduate students in a personal, experience-driven way.

## 9. References

- [1] Chua, L. O., "Memristor—The Missing Circuit Element", IEEE Transactions on Circuit Theory, CT-18 (5): 507–519, 1971
- [2] Strukov, Dmitri B.; Snider, Gregory S.; Stewart, Duncan R.; Williams, R. Stanley, "The missing memristor found", Nature, 453(7191): 80–3, 2008
- [3] Madou, Marc J., Taylor & Francis, Fundamentals of Microfabrication and Nanotechnology, Volume Two: Manufacturing Techniques for Microfabrication and Nanotechnology, Third Edition, CRC Press, July 2011
- [4] Terabe, K., Hasegawa, T., Nakayama, T., Aono, M. TI, Quantized conductance atomic switch, Nature 433, 47-50, 2005