

On the Development, Simulation and Testing of a Mixed-Signal Flash ADC with Application to a Digital Voltmeter

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Abstract

The basic idea of a mixed signal system is explored in this work. A Flash Analog-to-Digital Converter (ADC) is developed, simulated and tested. Absolute accuracy error, offset error, gain error and differential non-linearity (DNL) are some of the tests conducted with successful results. A simulated version of the developed Flash ADC system was used to correlate results.

1. Introduction

About 25 years ago, the circuit discussed in this paper was only known as an Analog-to-Digital Converter (ADC) – Data converter. The terminology “Mixed-Signal System” was not thought of at that time. A mixed signal system can be defined as the interfacing system that connects the analog and the digital subsystems in any communication system. In effect, it interfaces the analog “world” with the digital “world”. In this paper, the basic idea of a flash ADC system is explored in the context of a mixed signal system. ADC is an electronic device, often an integrated circuit that converts an analog voltage to a digital value. Some of the most popular ADC types are: The parallel or flash, or simultaneous converter, the successive approximation, and the voltage-to-frequency converter [1], [2], [3], [4], and [5]. Different types offer varying resolution, accuracy and speed specifications.

A Flash ADC is developed, simulated and tested. Absolute accuracy errors, Offset errors, gain errors and differential non-linearity (DNL) are some of the tests conducted with successful results. In Section 2, we discussed the Flash ADC basics, in Section 3; the application to a digital voltmeter is discussed. In Sections 4, 5 and 6 we discussed the computer simulation, the physical model and testing work done respectively. Sections 7, 8 and 9 are the conclusions, references and acknowledgements respectively.

2. Flash ADC Basics

The Flash ADC is the fastest and also the simplest of the ADC schemes [2], [3], and [5]. It is designed using a voltage divider connected to a series of comparators and an encoder. Figure 1 shows how the components in a flash converter are organized. It uses a reference voltage at the full-scale (FS) of the input range and a voltage divider. The latter is composed of $2^n + 1$ resistors in series, where n is the ADC resolution in bits. The value of the input voltage is determined by using a comparator at each of the 2^n reference voltages created in the voltage divider. Flash converters are very fast (up to 500 MHz or more) because the bits are determined in parallel. This method requires a large number of comparators, thereby limiting the resolution of most parallel converters to 8 bits (256 comparators). Flash converters are commonly found in transient digitizers and digital oscilloscopes.

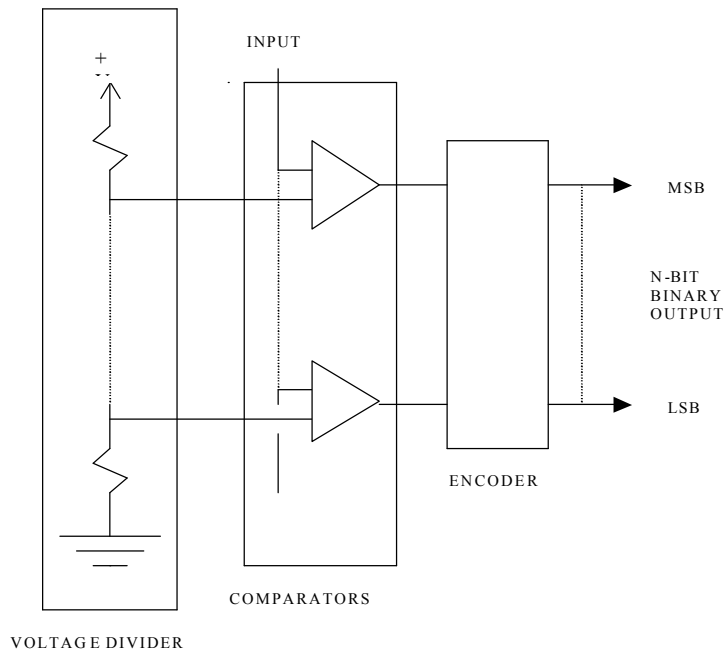


Figure 1: Block diagram of Flash ADC

The first stage of a Flash ADC is a standard voltage divider and its purpose is to divide the voltage so that each comparator has a different voltage at their input. The comparators compare each voltage of their inputs to determine an output of either high (1) or low (0) based on a set of threshold value. Finally, in this particular case, the encoder takes the output of each comparator and changes it to a true Binary Coded Decimal (BCD) form. It should be pointed out that not all Flash ADCs convert to BCD. In this work, we applied our application to a digital voltmeter.

3. Application to a Digital Voltmeter

A digital voltmeter is an instrument that measures the voltage of any low power circuit, and displays the value on a digital display. We decided to demonstrate the Flash ADC concept by building a single-digit digital voltmeter.

3.1 Defining the Components

Our process of design included defining the components that would be needed. The following is a list of the components:

- **Voltage Divider**

In order to design our voltage divider we needed a total of eleven 1 k Ω resistors. Since $I=V/R$, with an 11V input and 11 k Ω total, the current = 1mA. Therefore, each resistor drops 1V. The noninverting inputs of comparators one through ten are at 1V to 10V successively. See Table 1 for ideal and measured resistor values.

- **LM339N Quad Comparator**

The LM339N chip contains four comparators. For our design, we utilized three chips, which in total gave us the ten comparators we needed plus two, which were not utilized.

- **A 74147 10-to-4 Priority Encoder**

The 74147 encoder converts the output of the comparators to a true binary coded decimal (BCD) form.

- **A 7404 Hex Inverter**

Since the comparators and encoder are active low, we need an inverter to make each output active high. The 7404 Hex Inverter performed that function in our design.

- **A 7447 BCD to 7-Segment Decoder/Driver**

The 7447 BCD to 7-segment decoder/driver takes the BCD code and decodes it to drive the 7-segment decoder.

- **A NTE3068 Common Anode Seven Segment Display**

The seven-segment display takes the code from the decoder and displays the numerical value. The entire Flash ADC system was simulated using Multisim as shown in Figure 2.

Table 1: Resistor Values

Resistors	Ideal W	Actual W
1	1k	1.0006k
2	1k	.9980k
3	1k	.9978k
4	1k	.9956k
5	1k	.9983k
6	1k	.9964k
7	1k	.9970k
8	1k	.9976k
9	1k	.9980k
10	1k	.9984k
11	1k	.9983k

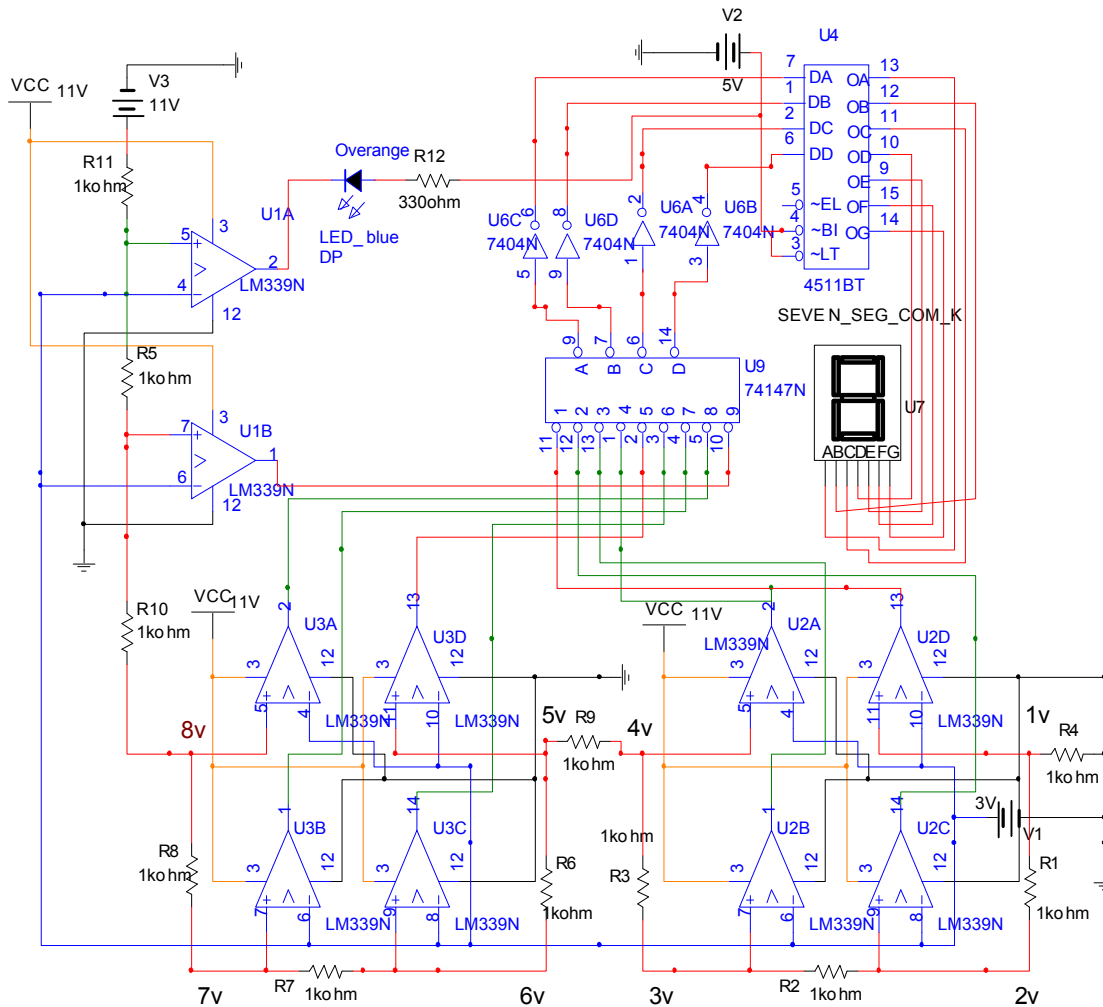


Figure 2: Multisim Simulation

4. Computer Simulation

After defining our voltage divider and the other components needed, we simulated the ADC system. We used Multisim, which is a software for circuit design, to build our digital voltmeter. Figure 2 shows the Multisim simulation and Figure 3 shows the designed circuit prototype. We used the simulated circuit to verify our design and intended application as a digital voltmeter. This allowed us to build the physical model (prototype).

5. Physical Model

Figure 3 shows the Flash ADC physical prototype model with application to a digital voltmeter that we developed and simulated to demonstrate the Flash ADC conversion method.

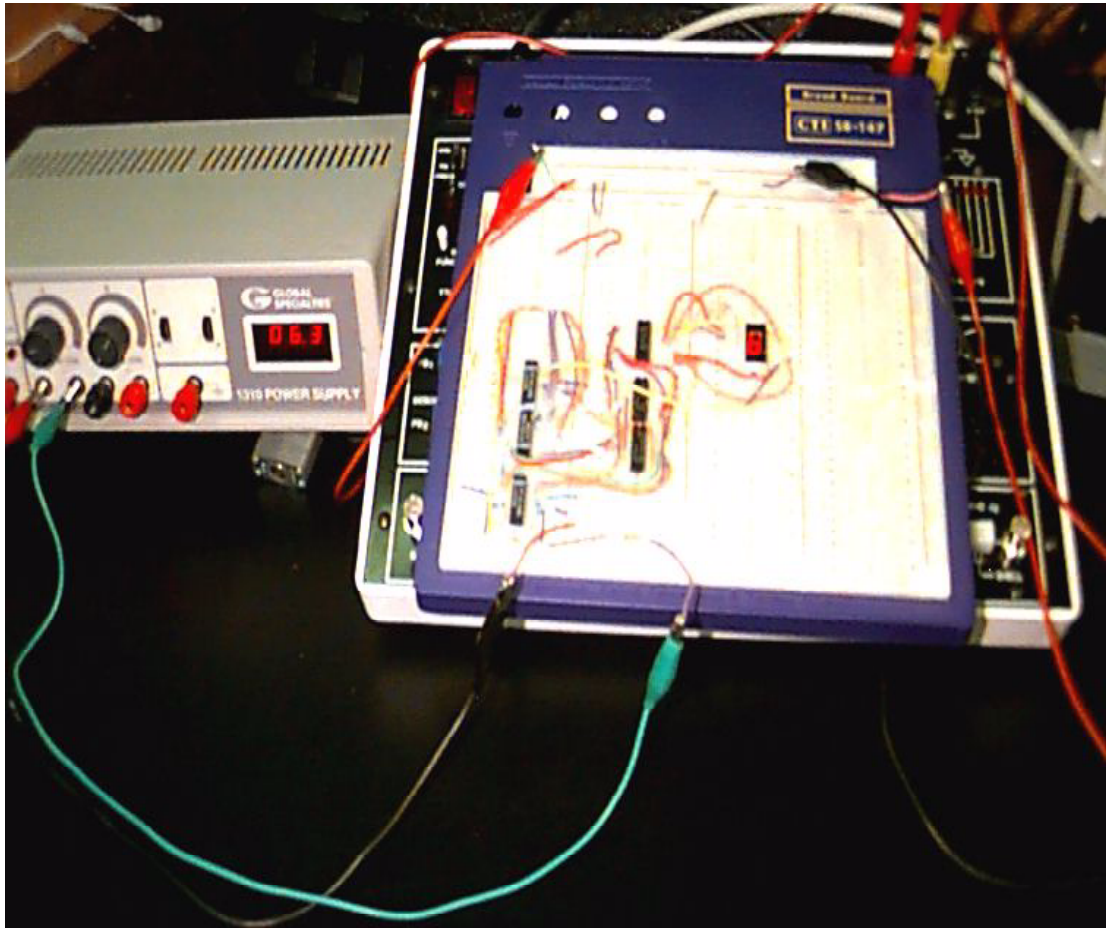


Figure 3: Developed Flash ADC Prototype

6. Testing of the ADC Mixed Signal System

Both the simulation and the physical prototype model enabled us to demonstrate the testing of some of the key parameters. Our test set up consists of our dc input ranging from 0-10V. We measured each major node of our circuit and compared each value to the expected value for each major node.

6.1 Absolute Accuracy Error

Absolute accuracy error is the difference between the theoretical analog input required to produce a given output code and the actual analog input required to produce the same code (See Tables 2 and 3). The actual input is a range and the error is the midpoint of the measured band and the theoretical band.

6.2 Offset Error

Offset error is the constant error or shift from the ideal transfer characteristic of the Flash ADC. In a Digital-to-Analog Converter (DAC), it is the output obtained when that output should be zero. In this Flash ADC, it is the difference between the input level that causes the first code transition and what that input level should be (See Figure 4).

Table 2: Active Comparator Voltages

Comparator	Ideal (V)	Simulation (V)	Actual (V)
1	1	1.1	1.023
2	2	2.1	2.081
3	3	3.1	3.115
4	4	4.1	4.143
5	5	5.1	5.160
6	6	6.1	6.201
7	7	7.1	7.216
8	8	8.1	8.249
9	9	9.1	9.281
10	10	10.1	10.301

Table 3: Comparing Voltage at the + Input

Comparator Node	Ideal (V)	Actual (V)
1	1	1.013
2	2	2.009
3	3	3.005
4	4	4
5	5	4.996
6	6	5.991
7	7	6.987
8	8	7.983
9	9	8.981
10	10	9.979

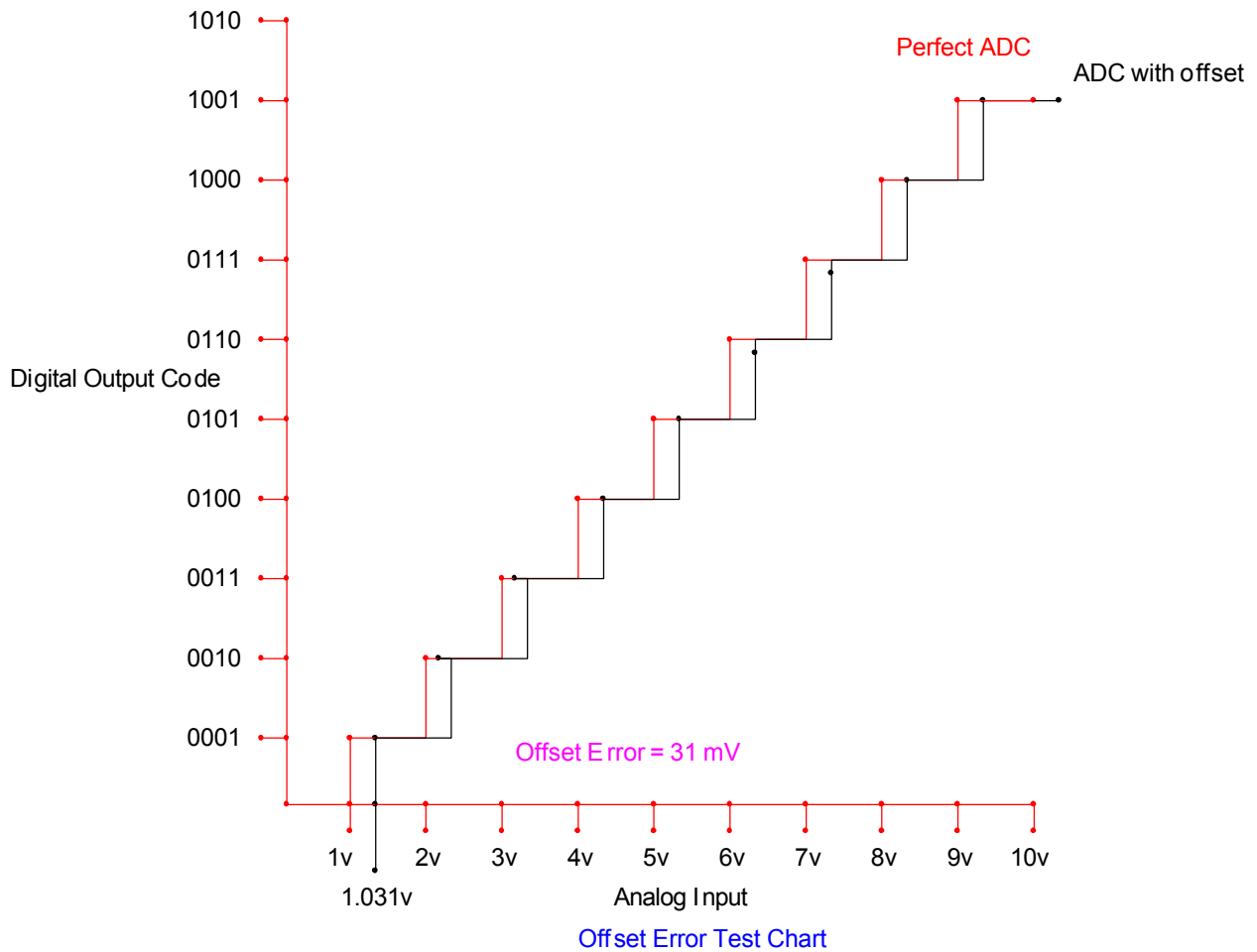


Figure 4: Ideal Transfer Curve Used in Testing for the ADC of Offset Error

6.3 Gain Error

Gain Error is the error of the slope of the line drawn through the midpoints of the steps of the transfer function as compared to the ideal slope. It is usually measured by determining the error of the analog input voltage to cause a full-scale output word with the ideal value that should cause this full-scale output. This gain error is usually expressed in Least Significant Bit (LSB) or in percent of full-scale range (See Figure 5).

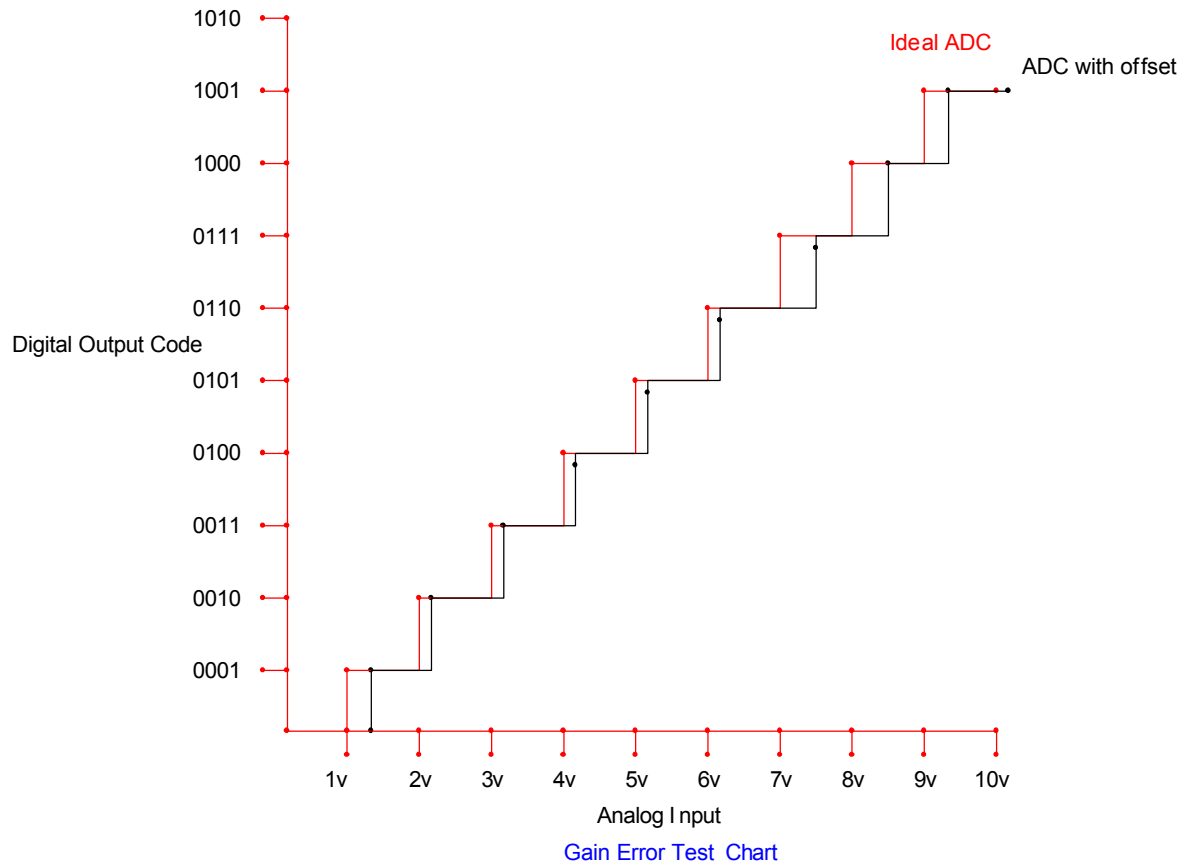


Figure 5: Gain Error Test Chart

6.4 Differential Non-Linearity (DNL)

DNL error is defined as the difference between an actual step width and the ideal value of 1LSB. For an ideal ADC, in which the differential nonlinearity coincides with $DNL = 0LSB$, each analog step equals 1LSB ($1LSB = V_{FSR} / 2^N$), where V_{FSR} is the full-scale range and N is the resolution of the ADC) and the transition values are spaced exactly 1LSB apart. A DNL error specification of less than or equal to 1LSB guarantees a monotonic transfer function with no missing codes. An ADC's monotonicity is guaranteed when its digital output increases (or remains constant) with an increasing input signal, thereby avoiding sign changes in the slope of the transfer curve. DNL is specified after the static gain error has been removed. It is defined as follows:

$$DNL = \left| \left[\frac{V_{D+1} - V_D}{V_{LSB - IDEAL} - 1} \right] \right|, \text{ where } 0 < D < 2^N - 2$$

V_D is the physical value corresponding to the digital output code D , N is the ADC resolution, and $V_{LSB-IDEAL}$ is the ideal spacing for two adjacent digital codes. By adding noise and spurious components beyond the effects of quantization, higher values of DNL usually limit the ADC's performance in terms of signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR). To guarantee no missing codes and a monotonic transfer function, an ADC's DNL must be less than 1LSB. To get the average LSB size, we first calculate the average code width. For Example:

$$\begin{aligned}
 V_{+fs} &= 10.301 \text{ V (code edge from 9 to 10)} \\
 V_{-fs} &= 1.031 \text{ V (code edge from 0 to 1)} \\
 \text{LSB} &= \text{Average Code Width} = (V_{+fs} - V_{-fs}) / 2^n - 2 \text{ volts} \\
 &= (10.301 - 1.023) / 9 \\
 &= 1.031 \text{ V}
 \end{aligned}$$

See Table 4 for our actual DNL values.

Table 4: Actual DNL Values

Codes	DNL
0 - 1	-0.039
1 - 2	0.0262
2 - 3	0.003
3 - 4	-0.003
4 - 5	-0.013
5 - 6	0.009
6 - 7	-0.015
7 - 8	0.002
8 - 9	0.001
9 - 10	-0.011

With our Average code width, we can now calculate the exact width of each code.

Table 5: Values of Exact Calculated Code Width

Code	Calculation	Code width (V)
1	1 * 1.031 V	1.031
2	1 * 1.031 V	1.031
3	1 * 1.031 V	1.031
4	1 * 1.031 V	1.031
5	1 * 1.031 V	1.031
6	1.25 * 1.031 V	1.29
7	1 * 1.031 V	1.031
8	.75 * 1.031 V	.773
9	1 * 1.031 V	1.031

Once we have our exact code width of each code, next we calculate the code edges used to reconstruct the transfer characteristic curve for our tests.

Code 1 = 1.031 V

Code 2 = 1.031 + 1.031 = 2.062 V

Code 3 = 1.031 + 2.062 = 3.093 V

Code 4 = 1.031 + 3.093 = 4.124 V

Code 5 = 1.031 + 4.124 = 5.155 V

Code 6 = 1.031 + 5.155 = 6.186 V

Code 7 = 1.290 + 6.186 = 7.476 V

Code 8 = 1.031 + 7.476 = 8.507 V

Code 9 = .7730 + 8.507 = 9.28 V

Code 10 = 1.031 + 9.28 = 10.311 V

According to our reconstructed transfer characteristic curve shown in Figure 6, we have very little errors in our DNL calculations, which translated to a good digital read-out – the Digital Voltmeter.

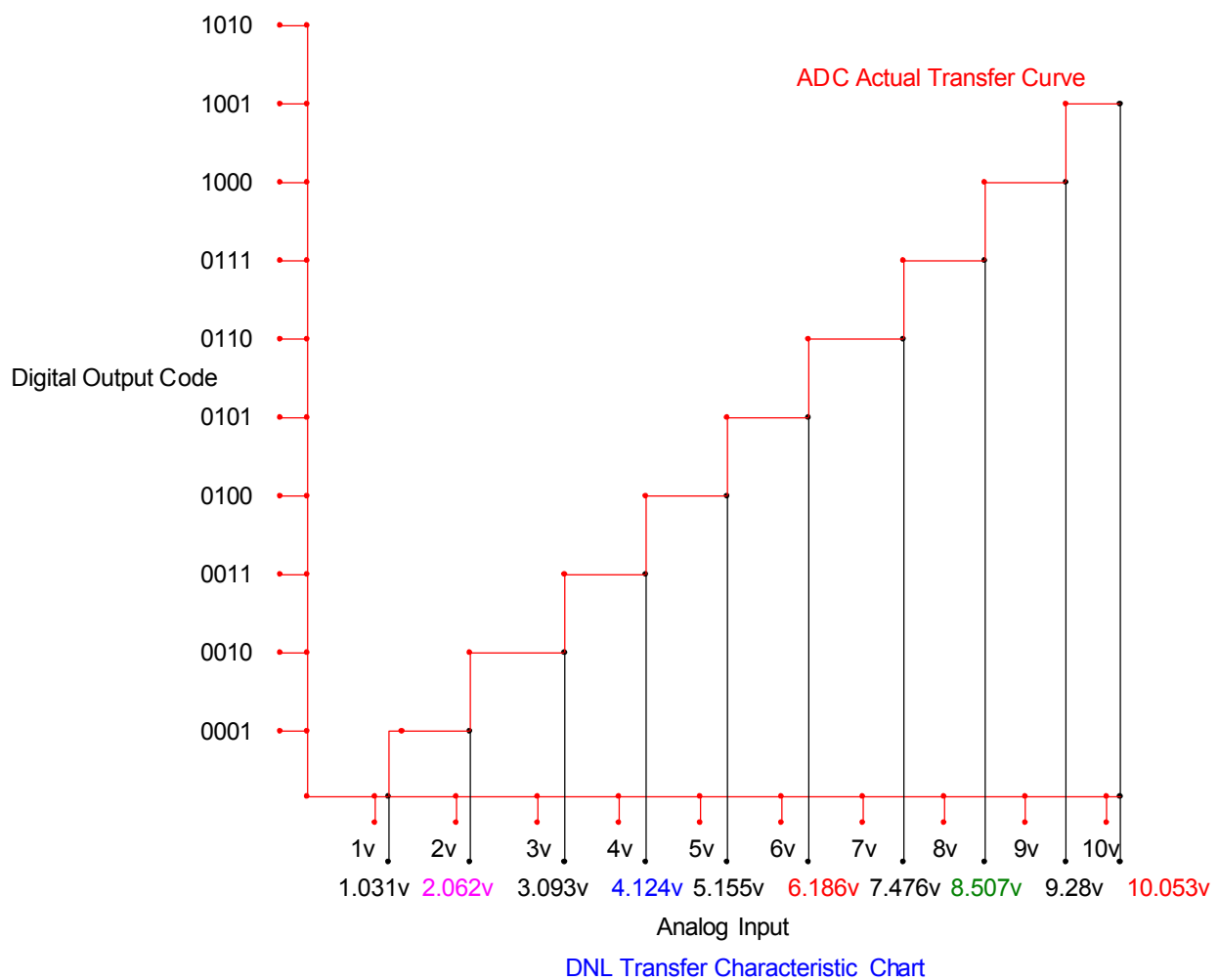


Figure 6: DNL Transfer Characteristic Curve

Conclusion

The concept of a mixed signal Flash ADC has been successfully developed, implemented and simulated. A working prototype was also built after being successfully simulated. The developed ADC Flash system was tested for absolute accuracy error offset error and Gain error. The results have shown that the developed system not only demonstrated the concept of an ADC Flash scheme but also demonstrated how it can be applied as a digital voltmeter. Future work on this will be to continue to perform other tests and to expand the read-out to have more than one digit reading.

7.0 References

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8.0 Acknowledgements

We want to acknowledge the contributions of Rodrigo Lozano, Richard Ellis and Ben Franklin in this work. They helped the author work on this project as part of their class research project. We extend our thanks to Texas Instruments for funding the Mixed Signal Systems Laboratory at Prairie View A&M University, Grant #s 410171 and 552207.

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Dr. Akujuobi is the founding Director of the Mixed Signal Systems Program and Laboratory at Prairie View A&M University. He is also the founding Director of the Center of Excellence for Communication Systems Technology Research (CECSTR). One of his research interests is in the area of Mixed Signal Systems. He is also one of the Researchers with the NASA Center for Applied Radiation Research (CARR).