AC 2011-1150: PHASE LOCK LOOP CONTROL SYSTEM LAB DEVELOPMENT

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Phase Lock Loop Control System Lab Development

Abstract

An important area in the field of electrical engineering is the study of phase lock loops, which are used in many applications such as frequency demodulation. Generally, the study of phase lock loops focuses on their implementation in communication systems using an LM565 chip or equivalent. However, phase lock loops can also be analyzed as a control systems problem. This paper presents the theory and analysis of phase lock loops and provides a description for showing how the frequency signal can lock into the reference signal. Simulation and experimental results validate the theoretical development, which allows for other instructors of control systems courses to incorporate a laboratory experiment in phase lock loops.

Introduction

The phase lock loop (PLL) is used extensively in electronic systems. For example, digital signal controllers use a PLL with an external oscillator to achieve a higher internal clock frequency[1]. The PLL is used in wireless communication systems for signal transmission and reception. It is used in demodulation of FM (frequency modulation) signals. It can also be used in noise rejection. The PLL is thus a valuable circuit in any application where precise control of a frequency signal is required.

Both analog and digital PLLs exist, depending on the application. The PLL has three basic components, as seen in Figure 1.

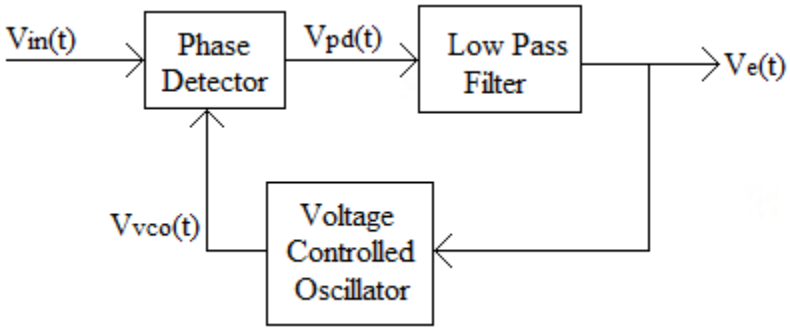

Figure 1. The Block Diagram of the Phase Lock Loop

An effective way to look at Figure 1 is to begin with the Voltage Controlled Oscillator (VCO). The VCO converts a dc input ($V_e(t)$) into a sinusoidal signal ($V_{vco}(t)$ with cyclic frequency f (Hz)) at the output. To accomplish a VCO by itself, one can use operational amplifiers if an analog VCO is desired, or using a numerically controlled oscillator if a digital VCO is desired. For the purposes of this discussion assume an analog VCO for an analog PLL is desired. Due to the feedback configuration of the VCO circuit, when the VCO is initialized, it will stabilize to its "free running frequency" (f_{vco}). The free running frequency can be affected by varying the input voltage to the VCO, namely $V_e(t)$.

The phase detector acts a multiplier of $V_{vco}(t)$ and $V_{in}(t)$, the input signal. When two sinusoidal signals are multiplied together, the resultant signal ($V_{PD}(t)$) will have two terms. The first term is a signal containing the difference in frequency between the two input signals. The second term is a signal containing the frequency sum between the two signals, due to a trigonometric identity[2]. This can be seen mathematically as follows:

$$V_{in}(t) = A_{in}\sin(\omega_1 t + \phi_{in}(t)) \quad \text{(Eq. 1)}$$

$$V_{vco}(t) = A_{vco}\cos(\omega_2 t + \phi_{vco}(t)) \quad \text{(Eq. 2)}$$

$$V_{PD}(t) = K_{PD}A_{in}A_{vco}\sin(\omega_1 t + \phi_{in}(t))\cos(\omega_2 t + \phi_{vco}(t))$$

$$= \frac{K_{PD}A_{in}A_2}{2}\sin((\omega_1 t - \omega_2 t + \phi_{in}(t) - \phi_{VCO}(t)) +$$

$$\frac{K_{PD}A_{in}A_2}{2}\sin(\omega_1 t + \omega_2 t + \phi_{in}(t) + \phi_{VCO}(t)) \quad \text{(Eq. 3)}$$

Where,

$V_{in}(t)$ is the input signal
A_{in} is the amplitude of $V_{in}(t)$
ω_1 is the radian frequency of Vin(t) (rad/s)
$\phi_{in}(t)$ is the phase angle of the input signal (rad)
$V_{vco}(t)$ is the VCO signal
A_{vco} is the amplitude of $V_{vco}(t)$
ω_2 is the radian frequency of $V_{vco}(t)$ (rad/s)
$\phi_{vco}(t)$ is the phase angle of the VCO (rad)
$V_{PD}(t)$ is the output signal of the phase detector
K_{PD} is a multiplier in the phase detector

Signal $V_{in}(t)$ is represented by a sine function and $V_{vco}(t)$ is represented by a cosine function. This acknowledges that a phase shift between the two functions will likely exist when the system is "locked" such that the frequencies ω_1 and ω_2 are equal. The size of the multiplier K_{PD} in the phase detector is chosen to help stabilize the system.

The low pass filter is designed to filter out the second term in Eq. 3, where the resultant sinusoidal signal from the phase detector includes the sum of $\omega_1 t$ and $\omega_2 t$. By choosing a filter that passes the difference in frequencies, i.e., term 1 of Eq. 3, and attenuates the sum of the two frequencies, i.e., term 2 of Eq. 3, the principal signal that gets inputted into the VCO is due to term 1. The whole system of Figure 1 is thus a feedback control system, and when the system is locked, the frequencies of $V_{in}(t)$ and $V_{vco}(t)$ are equal. In the locked state, Eq. (3) can be rewritten as:

$$V_{PD}(t) = \frac{K_{PD}A_{in}A_2}{2}\sin(\phi_{in}(t) - \phi_{VCO}(t)) + \frac{K_{PD}A_{in}A_2}{2}\sin(2\omega_1 t + \phi_{in}(t) + \phi_{VCO}(t)) \rightarrow \text{(Eq. 4)}$$

When these two frequencies (ω_1, ω_2) are the same, the phase difference between the two signals (i.e., $\phi_{in}(t) - \phi_{vco}(t)$) will also be constant. This is why the system is called a phase lock loop.

The error voltage $V_e(t)$ in Figure 1 is the output of the low pass filter and the input into the VCO. This error voltage can be determined in the locked state based on the phase difference between $\phi_{in}(t)$ and $\phi_{vco}(t)$, as seen in Eq. 5 below:

$$V_e(t) = 0.5K_{PD}A_{in}A_{vco}\sin(\phi_{in}(t) - \phi_{vco}(t)) \quad \text{(Eq. 5)}$$

As the phase difference between the two signals increases, the value of $V_e(t)$ will also increase because the sine function increases between 0° and 90°. The value of $V_e(t)$ may also be negative if the difference between the two phase quantities is negative.

To see how the PLL operates as a feedback control system, assume the system is in its locked state such that ω_1 and ω_2 are equal and a fixed phase difference $\phi_{in}(t) - \phi_{vco}(t)$ exists. If the input frequency ω_1 is increased, then the two systems will no longer be locked. Because the input frequency is now greater than the VCO frequency, the phase associated with the input signal will increase at a faster rate relative to the phase of the VCO. Thus, the phase difference $\phi_{in}(t) - \phi_{vco}(t)$ will increase. This increase in phase difference affects the error voltage $V_e(t)$ (see Eq. 5), causing it to increase as well. An increase in $V_e(t)$ causes the VCO to output a higher frequency, eventually reaching steady state at the new frequency of Vin.

The PLL has two ranges. The first range is called the capture range, and represents the range of input frequency ω_1 where the PLL is able to lock onto the signal from an unlocked state. The second range is called the tracking range, and represents the range of input frequency ω_1 where the PLL is able to maintain the lock on the input frequency. This is represented pictorially in Figure 2, and shows that the tracking range is broader than the capture range:

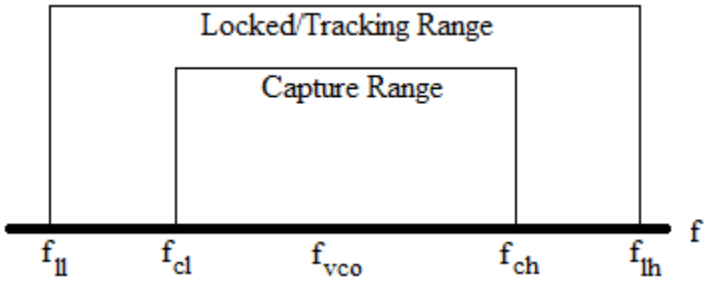

Figure 2. Phase Locked Loop Operating Ranges

Where,
f_{ll} = Low Locked Frequency Boundary (Hz)
f_{lh} = High Locked Frequency Boundary (Hz)
f_{cl} = Low Capture Frequency Boundary (Hz)
f_{ch} = High Locked Frequency Boundary (Hz)
f_{vco} = VCO Free-Running Frequency (Hz)

The PLL can be implemented inexpensively using an LM565 or 74HC4046 chip[3,4]. These chips typically include both the phase detector and the VCO. External resistors and capacitors are used to set the VCO free running frequency and implement the proper filter.

PLL System Model

A Simulink model of the PLL is presented in Figure 3.

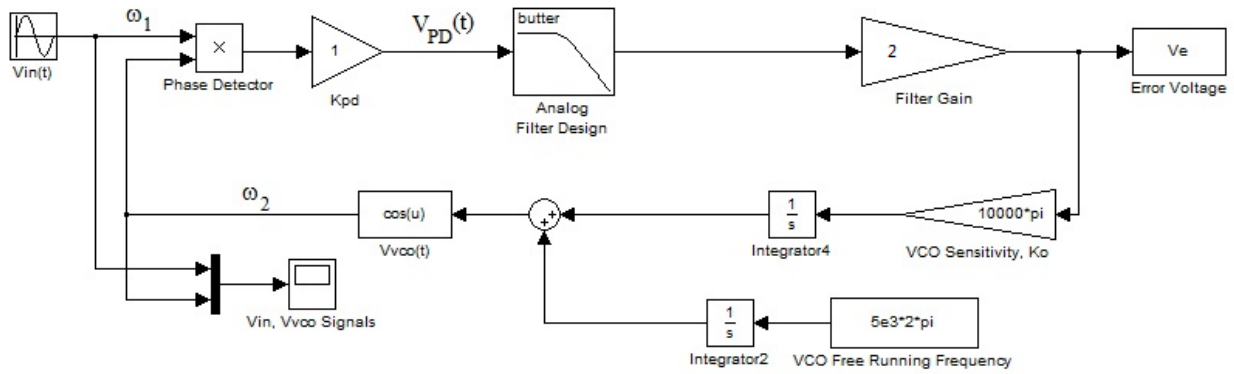

Figure 3. Simulink Model of a Phase Lock Loop

The system of Figure 3 is designed to lock onto a 10kHz input signal, $V_{in}(t)$. The VCO free running frequency is only 5kHz. Thus, the error signal $V_e(t)$ will need to provide a voltage signal that can yield an "additional" 5kHz of frequency out of the VCO. This is accomplished with an amplifier called the VCO sensitivity gain, K_o. Thus,

$$\omega_2(t) = \omega_o + K_o V_e(t), \qquad \text{(Eq. 6)}$$

Where ω_o = VCO free running frequency = 10000π rad/s, or f_o = 5000 Hz in this example.

In Figure 3, $K_o = 10000\pi$ rad/s/V = 5000 Hz/V. Thus, $V_e(t)$ will need to equal one volt to yield the proper frequency at the output of the VCO (10kHz). This is demonstrated in Figure 4. Note that the low pass filter is a 2nd order Butterworth filter with a pass band of 7 kHz. It is reasonable to assume that varying the filter design may further attenuate the higher frequency components still present from the second term of Eq. 3.

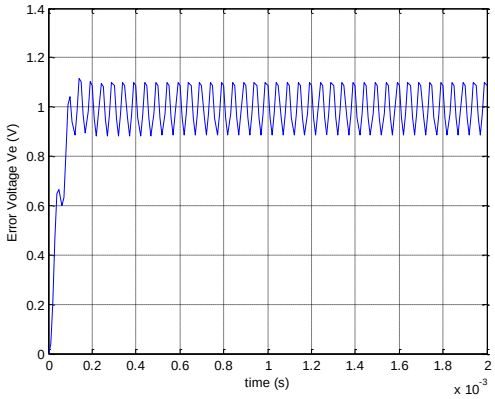

Figure 4. Plot of PLL Error Voltage (Ve) vs time

Figure 5 shows how the VCO is able to lock onto the input signal.

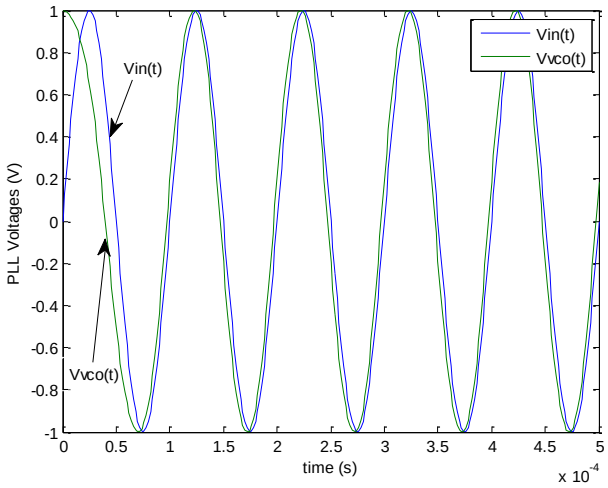

Figure 5. Plots of input voltage and VCO voltage versus time

The overall loop gain of the phase lock loop is also an important consideration. This gain is equal to the product of the gains for the phase detector, low pass filter, and sensitivity gain, K_o. The filter gain is iteratively chosen to be 2 to reduce the amplitude of the noise in the error voltage signal. Loop gains should be chosen carefully, or the PLL will not lock.

PLL Control System Analysis

When analyzing the PLL as a control system, it is first assumed that the PLL has already locked onto the input signal[5]. This helps to simplify the analysis, as will be seen. Referring back to Figure 1 and Eq. 2, if there is a frequency change in V_{vco}, then this change is due to a change in the error voltage Ve. This might be written mathematically as:

$$\Delta f_o = K_o V_e(t) \qquad \text{(Eq. 7)}$$

Where Δf_o = the instantaneous change in frequency (Hz) of V_{vco}

Equation 7 assumes a linear VCO characteristic, i.e., the VCO frequency changes linearly with changes in V_e. The changing frequency $f_o(t)$ is then a function of the prior (locked) frequency plus the instantaneous change, namely:

$$f_o(t) = f_o + \Delta f_o = f_o + K_o V_e(t) \qquad \text{(Eq. 8)}$$

The phase angle of the VCO, $\phi_{vco}(t)$, due to the instantaneous change in frequency is represented as an integration of the instantaneous frequency change, or:

$$\theta_o(t) = 2\pi\int f_o(t) = 2\pi f_o t + \theta_o + 2\pi K_o \int V_e(t)dt \qquad \text{(Eq. 9)}$$

Note that the first two terms represent the phase angle based on the constant VCO frequency f_o. Thus Eq. 9 indicates the VCO phase angle operates on the integral of the error voltage $V_e(t)$.

A basic block diagram of the PLL in the locked condition is shown in Figure 6. Based on the prior discussion, the VCO is represented by an integrator in the Laplace domain. This makes the PLL a first order system without considering the type of filter (F(s)) employed. If a 1st order low-pass filter is employed, then the PLL in the locked condition becomes a 2nd order system. One approach[6] is to employ a phase lag compensator to help mitigate stability issues. In such an approach, the zero cutoff frequency (ω_z) would be located at the geometric mean between the pole cutoff frequency (ω_p) and the value of the overall loop gain ($K_{pd}K_aK_o$), where K_a is the dc gain of the filter. Mathematically, this would be written as:

$$\omega_z = \sqrt{\omega_p K_{PD} K_a K_o} \qquad \text{(Eq. 10)}$$

However, any appropriate filter may be used (such as the 2nd order Butterworth filter used earlier) as long as the filter removes the high frequency components while passing the low frequency components and ensuring stability of the overall system.

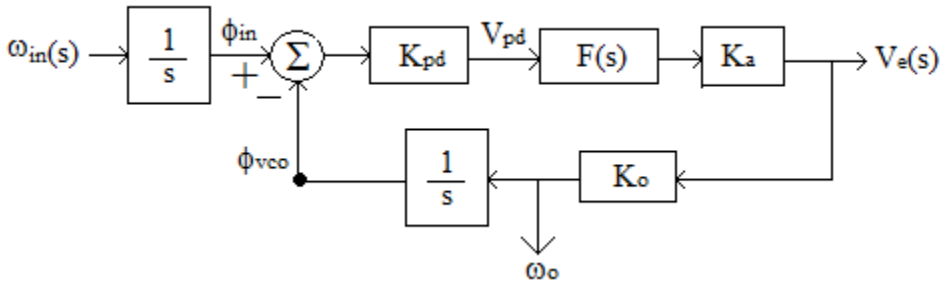

Figure 6. Block diagram of the PLL in the locked condition

Experimental Results

Electrical and computer engineering technology students, working in teams of two, were tasked to construct a PLL using its basic blocks from Figure 1 and determine its capture and tracking ranges. Each student team worked at a station that has the following equipment at their disposal:

- Triple Output Dc Power Supply (0-6V,±0-25V)
- Function Generator
- Digital Multimeter
- Digital Oscilloscope
- Frequency Counter

To help simplify the construction, the PLL was used to lock onto a square wave signal with 50% duty cycle. This requires two changes from the simulation of the previous section. First, an exclusive-or (XOR) gate (74HC86) was used as a Type 1 phase comparator versus the use of an

analog phase detector[6]. Second, the voltage levels needed to be adjusted such that only positive voltage levels were provided into the XOR gate.

The XOR gate will output a logic high when only one input is high, otherwise the output is logic low (Table 1). If the input signal (V_{in}) and the VCO signal (V_{vco}) are in phase the output will always be a logic low. On the other hand if the signals are 180° out of phase, the output will always be a logic high.

Table 1. XOR Truth Table

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

Figure 7 shows the simple operation of the XOR gate as a phase comparator. Note that the pulse width of the output signal depends on the phase difference between V_{vco} and V_{in}.

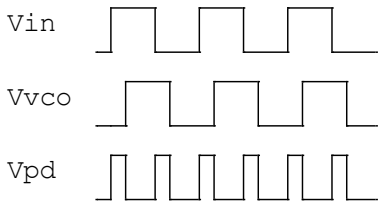

Figure 7. Phase Comparator Operation

The average dc voltage of the resulting phase detector signal (V_{pd}) is equal to the phase difference between the two input signals. Mathematically the average dc voltage (V_e) can be represented by the following equation:

$$V_e = V_{peak} \cdot D \qquad \text{(Eq. 11)}$$

Where,
V_{peak} = Peak value of V_{PD}
D = Duty Cycle

The R-C filter for this circuit is responsible for outputting the average dc voltage from the phase comparator signal V_{pd}. It is a simple R-C configuration which allows the PLL to be implemented without spending undue time designing the appropriate filter. The time constant was chosen such that a smooth gradually changing error voltage was produced. The R-C filter used in the laboratory experiment had a time constant of .11s ($500\Omega \; x \; 220\mu f$). Figure 8 illustrates the error voltage produced from the PSpice simulation for this circuit.

For the laboratory experiment, two circuits were constructed. The first circuit is shown in Figure 9, and uses LM741 operational amplifiers (op-amps) with the negative power supply input grounded.

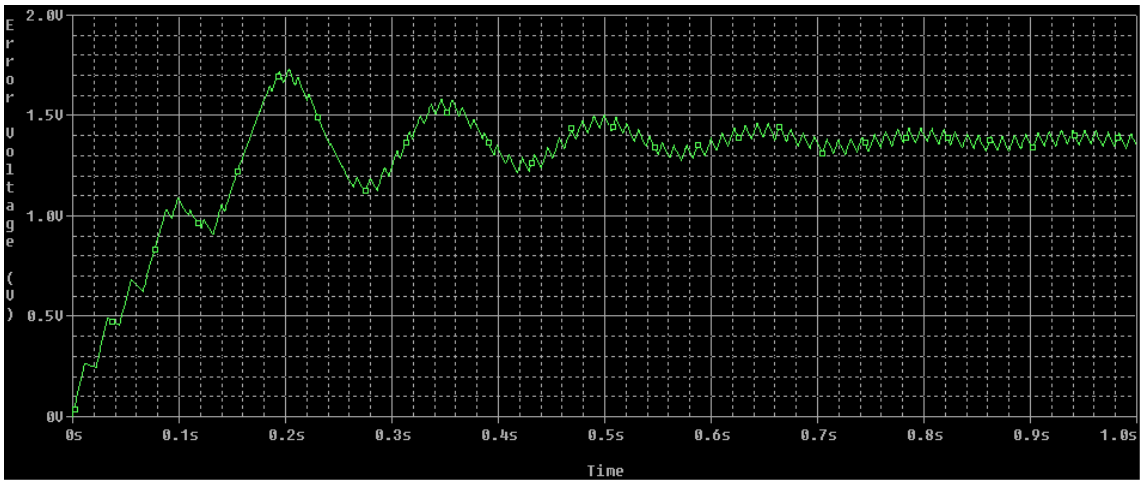

Figure 8. Error Voltage from the PSpice Simulation

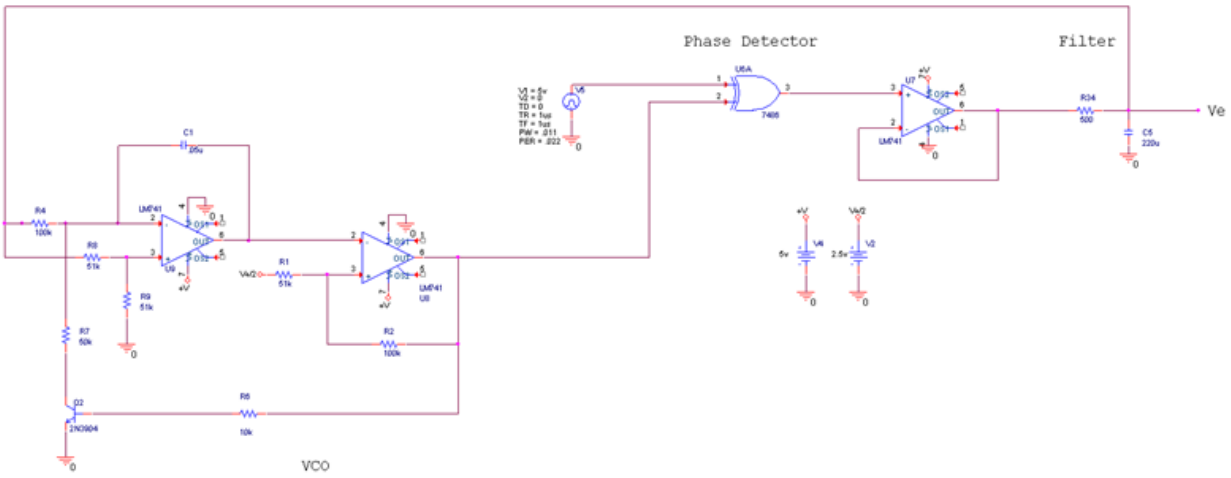

Figure 9. First PLL Circuit Schematic

Results for the capture and tracking ranges (see Figure 2 above) using this circuit are provided in Table 2. Results for teams 1 and 3 were similar, while those for teams 2 and 4 were similar. However, the results overall showed a wide disparity, and teams 2 and 4 had difficulty getting their PLL to work. Teams 2 and 4 also yielded lower capture and tracking ranges.

Table 2. Results from Student Construction of the PLL

	Lower Tracking Frequency	Lower Capture Frequency	Higher Capture Frequency	Higher Tracking Frequency
Team Number	f_{ll} (Hz)	f_{cl} (Hz)	f_{ch} (Hz)	f_{lh} (Hz)
1	16	40	72	114
2	18	26	43	60
3	20	37	81	105
4	13	16	41	56
5	21	36	67	105
6	18	47	81	127

Team 5 used a similar circuit but decided to forego using the LM741 op-amps and instead used one LM324 quad op-amp[7]. The LM324 requires only a single voltage supply versus the dual voltages required by the LM741, although it can be configured as a dual supply chip. The LM324 op-amps for this application are being powered via a single +5V supply in order to enusre that the voltage levels are kept within TTL tolerances. It should be stated that the VCO frequency obtained using the LM324 does not have a rail-to-rail output, therefore the actual output square wave may fall somewhere between this 0-5V range. In effect, this voltage difference alters the resulting frequency of the VCO signal (V_{vco}). The rail-to-rail output frequency of the VCO signal can be calculated as follows:

$$f = 3V_e/(4VRC) \quad \text{(Eq. 12)}$$

Where,
V_e = Error Voltage (V)
R = 100kΩ
C = .05μf
V = 5V

For example Table 3 shows the calcuated, simulated, and measured VCO output characteristics for an input (V_e) of 2.5V.

Table 3. Comparison of VCO Output Signals for V_e of 2.5V

	Vmin (V)	Vmax (V)	Frequency (Hz)
Calculated	0	5	75
PSpice	0	4.3	84
Measured	0	3.9	116

A difference in VCO frequencies can clearly be seen from the different methods used in in Table 3. However, the calculated frequency again assumes a rail-to-rail voltage at the output of the VCO, and this was not achieved with either Pspice or hardware. When the peak-to-peak voltage is less than the rail-to-rail voltage, the reduced amplitude square wave voltages tend to yield higher VCO frequencies. The rationale for this is not clear, but the results of Table 3 make more sense when the frequency of the signals are adjusted based on the reduced peak-to-peak voltage observed relative to the rail-to-rail voltage. For the PSpice results:

$$84Hz(4.3V/5V) = 72.24Hz \quad \text{(Eq. 13)}$$

The PSpice value (72.24Hz) now lines up closer with the calculated value (75Hz), a 3.7% difference. For the measured results:

$$116Hz(3.9V/5V) = 90.48Hz \quad \text{(Eq. 14)}$$

This now results in approximatley a 20.6% error.

Results for team 5 were similar to those of teams 1 and 3. However, team 5 also had issues making the PLL work properly with the circuit of Figure 8. Team 6 at a later date then worked on a revised approach, shown in Figure 10. This team was not available during the specified lab period, and this gave the lab instructors time to revise the circuit in hopes of making it more robust. Specifically, the buffer op-amp was moved from the output of the phase comparator to the output of the VCO. Results for team 6 were similar to those of teams 1, 3 and 5, but without any circuit construction issues. The new circuit widens the tracking range and maintains a reasonable capture range. It also only requires two chips (LM 324 quad op-amp, XOR), along with a simple R-C filter and a transistor. Yet this circuit still clearly delineates the major blocks of the PLL (VCO, phase comparator, filter).

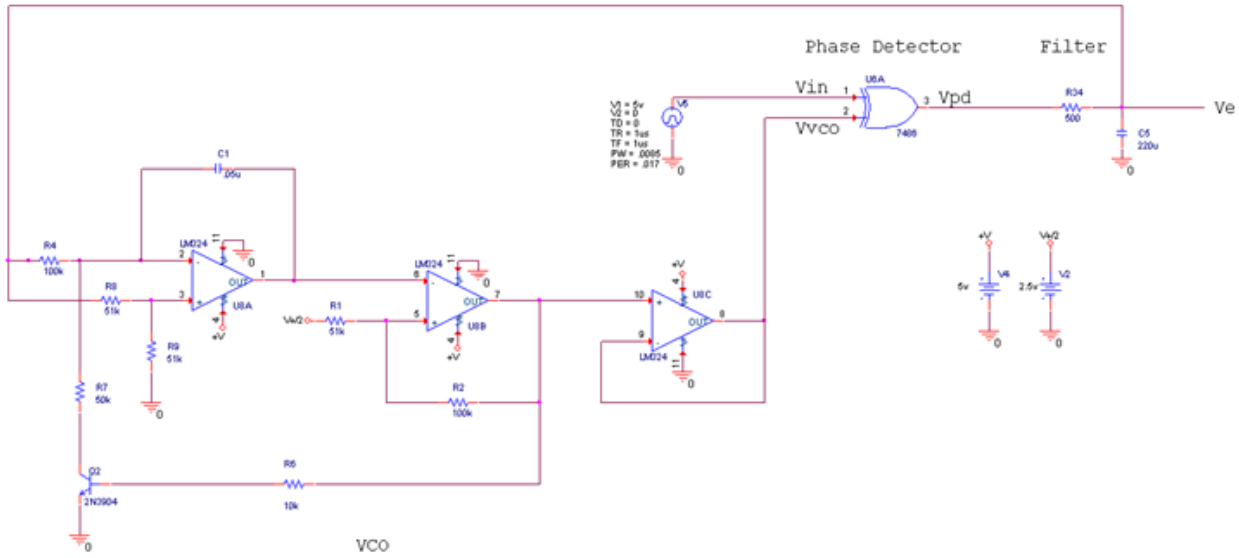

Figure 10. Revised PLL Circuit Schematic.

Student Assessment

Overall, the students felt this was a reasonable and effective lab, and only wished that more of the theory and design of the PLL were presented prior to beginning the lab. Typical comments include:

"*The phase lock loop lab was a very interesting lab. It provided much insight on how some radio oriented systems work. The lab was not too difficult and was not too easy either. Overall, the lab was well prepared and worked well once some kinks were worked out. The kinks in the lab were not a big deal, very minor inconveniences; however they are more of a learning experience more then anything else. I thought the schematic to build the system was well laid out and provided a very simple and easily understood way to construct the circuit.*"

"*This lab was a nice addition to learning about systems' phase characteristics. It introduced VCO's and thoroughly taught about phase locked loops (PLL) without complicated circuitry. You could view each state of the PLL and analyze how it was operating to the circuits design. Overall I feel this was an informative lab that was not too difficult but not terribly easy either.*

With a better developed lab instructional hand out and perhaps some expansion with changing the range or other characteristics of the PLL, this lab could be even more helpful and fun to work with."

Conclusion

In this paper a phase lock loop is presented as a control system topic. The PLL has a significant amount of complexity, and the emphasis here is on providing a basic understanding of how the PLL works, and how a simple PLL can be constructed out of its principal components within a 2-hour laboratory period. The key advantage of this laboratory experiment is its ability to have students construct the PLL out of its principal components, versus simply using an integrated circuit. The experimental results from student teams showed the viability of implementing this circuit, and the improved circuit should reduce the amount of troubleshooting required. Student comments indicate that the laboratory handout should include more background information, and the information provided in this paper should help in that regard.

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