Protecting and Enhancing the M68HC11 for Student Use

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Abstract

The teaching of microprocessors to undergraduates poses many problems. The least of these, at the introductory level, should be inconsistencies or difficulties in running simple experiments on the microprocessor itself. This paper presents the development efforts at the Milwaukee School of Engineering (MSOE) to develop a modular platform for the teaching of the M68HC11 microprocessor. Central to this is a M68HC11EVB2 trainer board packaged in an attache case with a power supply, a buffering board for protection, and an external development platform that supports access to the ports of the M68HC11 and provides convenient interfaces to common I/O devices. An unique feature of this system is that the buffer board provides transparent buffering of the many bi-directional I/O pins of the M68HC11. The effects of using this new system will be examined with emphasis on repair and replacement of damaged units. Additionally the efforts to adapt a M68HC11EVB board to this system will be presented.

Introduction

There is no question that we are firmly implanted into the era of the computer. It is almost impossible to by any type of electrical consumer product that does not contain at least one microprocessor. This runs the gamut from products as simple as toasters to as complex as the automobile. Consequently it is becoming more important for engineers, in all fields, to have at least a passing knowledge of microprocessors and embedded systems. This is no more evident than in the curriculums at MSOE. Not only are embedded systems taught throughout the computer engineering curriculum (from assembly language in the sophomore year to their role in networks in their senior year) but they also play a prominent role in the sophomore year of our electrical engineering and electrical engineering technology programs as well as service roles in the mechanical engineering (junior) and mechanincal engineering technology (sophomore) programs. The requires a significant investement in infrastructure. This paper will discuss the goals of the MSOE development of this infrastructure and examine its success. It will also discuss our efforts to adapt this infrastructure to changing microprocessor boards.

Goals

Due to the varied nature of MSOE's courses in microprocessors and embedded systems, we set the following goals for our development platform.

1) Readily portable - ideally the platform should consist of very few parts/pieces
2) Usable with any PC - this simplifies scheduling of courses between any of various PC labs

3) Robust - continual problems with repairs and malfunctions are costly and frustrating to the students
4) Easy to use - various common I/O devices should be included as part of the system as well as access to a prototyping area
5) Exchangable - any student circuitry should be easily attachable and detachable from the platform to allow the isolation of one student's experiment while another uses the microprocessor

The Initial Attempt

For years MSOE had been using a Z80-based development platform that supported many of these goals. It provided a serial connection to a PC, many common I/O devices (for Z80 systems), and a prototyping area. Over the years these boards served us well, but eventually they started to breakdown, the Z80 declined in popularity, and many of the system's limitations resulted in our decision to move to a more modern processor.

One of the more popular microprocessors/microcontrollers at that time and today is the Motorola M68HC11. It has many of the common embedded system features and Motorola has always provided excellent university support through donations and development tools such as AS11, BUFFALO, and PCbug11. Additionally we received a donation of a number of M68HC11EVB2 microprocessor boards from Motorola which not only included the M68HC11 with a port-replacement unit, but also include the Georgia Tech companion logic analyzer board.

Due to lack of proper development time we chose to temporarily bundle the M68HC11EVB2 in a case with a power supply for student use in our electrical engineering curriculum only. (The computer engineering students had already been using the simpler M68HC11EVBU in a stand-alone car project.) During that first term of use we found it very difficult for the students to wire in their own simple hardware. Additionally we were forced to replace at least eight (8) of the port-replacement units which had been damaged due to careless wiring. This was unacceptable.

The Host Suitcase and the Development Board

A development effort then followed based on the five goals listed above. The result was a two unit system which met all of these goals. The central unit is the host suitcase shown in Figure 1. This suitcase at first appears little different than the initial system with one primary exception. A buffer board was added to the system to provide the following:

1) Protection and buffering of the M68HC11 and the port-replacement unit
2) Easy access to all the bus pins
3) Addition of a mode switch to support both BUFFALO and PCbug11

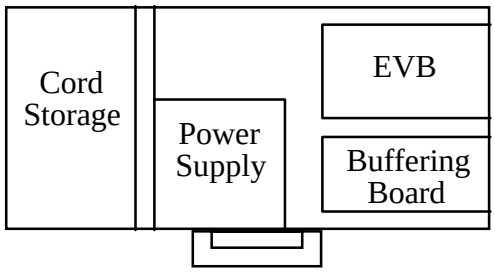

Figure 1 - Layout of the Host Suitcase

At an initial glance this would appear to be a simple board to develop until you realize that many of the I/O ports on the 68HC11 are bi-directional and that the bi-directionality is controlled at the pin-level not the nibble- or byte-level. And while bi-directional buffering is not particularly difficult doing so at the pin-level cannot be done using MSI TTL parts. The entire key to the system has to do with the way that the M68HC11 requires the programmer to set the direction of each pin. In order to control the direction of a pin a program must write to one of three *internal* registers, DDRC, DDRD, and PACTL. Fortunately the M68HC11 uses a memory-mapped I/O architecture that results in each of these writes appearing on the external address and data bus. A programmable logic device (PLD) was used to exhaustively decode these writes and trigger latches to store the direction of each pin as shown in the circuit of Figure 2. This also has the advantage of being completely transparent to the programmer so that the system is used exactly the same way as an unbuffered M68HC11 system. Over the last three years the number of parts damaged on the buffer boards has been limited to only a handful of cheap TTL parts; this is a vast improvement on our trial run with the original system.

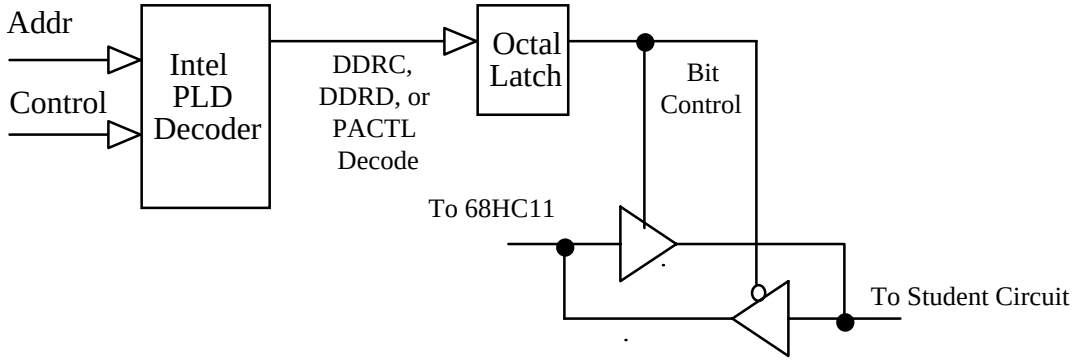

Figure 2 - The Bit-level Bidirectional Buffer Circuit

Note: This circuitry is not applied to PD0 and PD1 so as not to interfere with the operation of the SCI nor is buffering used on Port E which would interfere with the A/D subsystem.

The second component of the system is a development platform that connects to the buffer board using a cable and connector that also doubles as an in-circuit emulator for M68HC11s in single-chip mode. This platform is shown in Figure 3. To simplify early experiments and exercises with the M68HC11 this platform provides dedicated wiring to a 4x4 keypad (Port C) and a 4-character ASCII display which conveniently works with the strobed output mode of the M68HC11. Additionally there is a large prototype-area as well as protoboard-style connectors to all of the M68HC11 port pins as well as to interrupt system, DIP and momemtary switches, and a bank of standard LEDs. This provides for a wide variety of experimental options from simple light flashers to more complicated motor drivers. The detachability of the platform makes it use optional in software-only experiments and allows students to detach their project from the microprocessor so that another student may use it.

Other Development Efforts

A number of other development efforts have also been undertaken at MSOE to foster instruction of the M68HC11. Among the development efforts are:

1) The AS11 assembler has been enhanced to make its use simpler
2) The PCbug11 Talker has been modified for use in the M68HC11EVB2
3) Simple plug-in boards have been developed for DC motors, stepper motors, D/A converters, and ultrasonic range sensors
4) Development of APIs to use the DUART resident on the M68HC11EVB2

These provide plenty of flexibility to support the different needs of the various microprocessor courses at MSOE and the varing styles of individual faculty.

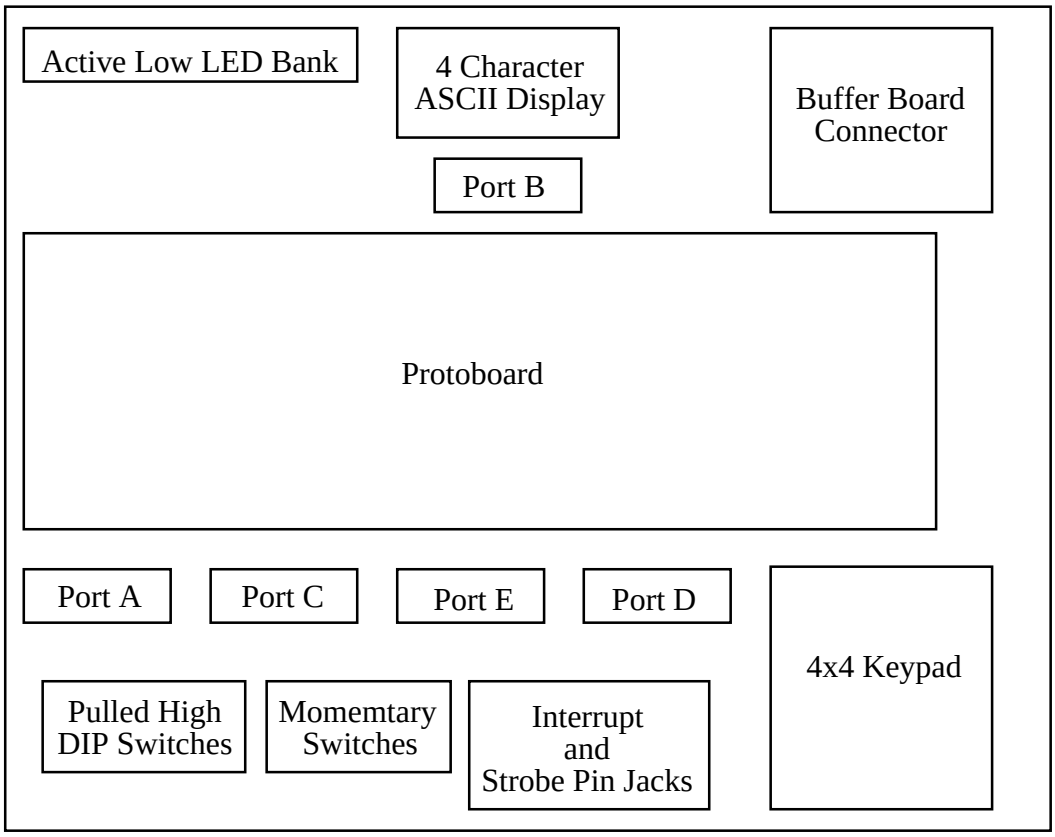

Figure 3 - Layout of the Development Platform

The M68HC11EVB

Unfortunately the M68HC11EVB2 is no longer available and in order to expand our microprocessor infrastructure we have had to change the central component of our system to the M68HC11EVB. To minimize the impact on students and professors alike we chose to alter the memory map and reset circuitry of the M68HC11EVB to allow its use with the current buffer board and development platform. This turned out to be possible with a minimum of modification to the M68HC11EVB board by removing its address decoder circuit (based on a 68HC138) and

inserting a piggy-back board into the decoder and one of the memory sockets (see Figure 4). This piggy-back board uses a single PLD to completely change the memory map of the M68HC11EVB to the M68HC11EVB2 and also includes the functionality of the buffer-board PLD.

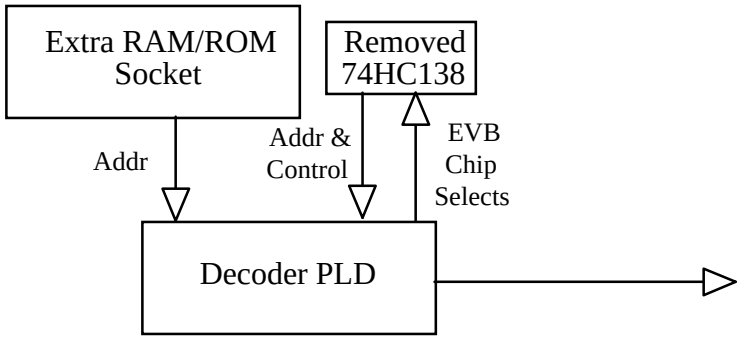

Figure 4 - The M68HC11EVB Piggy-back Decoder

Conclusions

The switch from the Z80 to the M68HC11 at MSOE has been very successful. This is due in large part to the development of a number of units and tools which makes the use of the M68HC11 both convenient and relatively trouble-free. Not only do these platforms operate with very few problems and failures they also support a wide-range of course requirements and instructor styles.

References

[1] Welch, H. and Sebern, M., *MSOE M68HC11 Microcontroller Technical Reference*, MSOE, 1995 & 1998.

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Biography

Dr. Henry L. Welch is an Associate Professor of Electrical Engineering and Computer Science at the Milwaukee School of Engineering. He earned his Ph.D. in Computer and Systems Engineering from Rensselaer Polytechnic University in 1990. His primary teaching areas are in digital circuits, microprocessor systems, and advanced computer engineering topics such as computer graphics and fuzzy logic.