Research Experiences for Women Undergraduate Students in High-Speed Integrated Circuits

Ashok Goel, Martha Sloan, Sarah Bergstrom, Aleli Mojica-Campbell, Stephanie Draeger, Lehang Huynh, Jami Meteer, Rebecca Morrison and Stephanie Weitemeyer

Department of Electrical Engineering
Michigan Technological University

Abstract

In this paper, the research projects carried out by the women undergraduate students selected for the NSF funded undergraduate summer research sites established at the department of Electrical Engineering at Michigan Technological University in the areas of design, modeling and simulation of GaAs-based very high-speed integrated circuits are outlined.

I. Introduction

It is widely accepted that active research experience is one of the most effective techniques for training and motivating undergraduate students for careers in science and engineering. National Science Foundation (NSF) recognizes this and supports undergraduate research under two “Research Experiences for Undergraduates” (REU) programs: a) Under their “REU Supplements” program, NSF encourages principal investigators of NSF-funded research grants to include one or two undergraduate students in their existing projects; b) Under their “REU Site” program, NSF provides funds to set up undergraduate research sites consisting of nearly ten students to work on state-of-the-art research projects under the supervision of a faculty member.

Recent advances in the integrated circuit technology have resulted in smaller transistor dimensions, larger chip sizes and increased complexity. There is an increasing demand for circuits with higher speeds and higher component densities. Because of its semi-insulating property and the fact that the mobility of electrons is an order of magnitude higher in Gallium Arsenide (GaAs) substrate than in the widely used Silicon substrate, GaAs has emerged as a preferred substrate for the development of very high-speed integrated circuits. In fact, during the last few years, GaAs technology has emerged rapidly from basic research to device and circuit development. In addition, growth of GaAs on silicon (Si) substrate has met with a great deal of interest because of its potential applications in the new hybrid technologies. GaAs-on-Si unites the high speed and optoelectronic capability of GaAs circuits with the low material cost and superior mechanical properties of the Si substrate. The heat sinking of such devices is better since the thermal conductivity of Si is three times more than that of GaAs. This technology is expanding rapidly from material research to device and circuit development. Functional GaAs SRAMs of up to 1K in complexity have been demonstrated on Si sub-

strate. LED modulation rates up to 27 Mbit/s have been demonstrated on monolithically integrated GaAs/AlGaAs LEDs and Si MOSFETs. Further, it may be recalled that CRAY-4 supercomputer is based primarily on the GaAs-based high-speed circuits. In this paper, an undergraduate research site on GaAs-based high-speed circuits set up at the Michigan Technological University is described and the research projects carried out by the women undergraduate students are summarized.

II. Undergraduate Research Sites

During summers of 1997, 1998 and 1999, funded by a 3-year grant from the National Science Foundation, undergraduate research sites were established at the department of Electrical Engineering at Michigan Technological University (MTU) in the area of GaAs based very high-speed integrated circuits. Each of these sites consisted of ten undergraduate students selected from institutions all over the USA. Eligibility criteria were:

a) citizenship or permanent resident of the United States; and
b) completion of at least two years in electrical engineering, computer engineering or a related field with a grade point average of 3.0 or over.

Major objectives of the REU site were:

a) enhancement of student experience, competence, confidence and self esteem by working on a state-of-the-art electrical engineering research project;

b) encouragement of students to pursue graduate studies in electrical engineering and to choose a career in microelectronics/VLSI research; and

c) improvement of student oral and written skills through written report and formal presentations.

NSF strongly encourages the inclusion of women students and students belonging to other under-represented groups to their REU sites. These three sites at MTU included eight women undergraduate students selected on a competitive basis. In addition to the host institution, women students were selected from the University of Notre Dame, University of Texas at El Paso, Swarthmore College, Michigan State University, Rutgers University and Calvin College. These students worked with electrical engineering graduate students and faculty members for ten weeks on projects ranging from designing GaAs-based circuits using MAGIC and L-Edit[1] to modeling the very high-frequency effects in the VLSI interconnections[2] to the study of electromigration-induced failure effects in the GaAs-based VLSI interconnections[2] to computer simulations of GaAs- and SOI-based devices using the semiconductor technological computer aided design (TCAD) tools. Interaction with the faculty and graduate students working in these areas was maximum during the first few weeks and decreased gradually as students became more and more independent in carrying out their projects. During the last week of the REU site, students submitted formal detailed written reports and presented formal seminars on their projects[3].

Graduate student Terrence Tan talking to the REU students

III. Undergraduate Projects

REU students realized that, while for the past few decades, silicon-based technologies have been used to fabricate integrated circuits, the limits of silicon are being reached as the end of the millennium approaches and new materials must be investigated to continue the aggressive growth demanded by consumers and modern industry. They found that GaAs is considered a prime candidate for designing components with high speed and modest power consumption due to its high electron mobility, high switching speed, low capacitances and high packing density. Therefore, to illustrate and test the feasibility of GaAs-based components, they designed several GaAs-based circuits using the CAD tool called MAGIC in conjunction with the GaAs technology files created by Long and Butner[1]. These circuits included a GaAs-based digital clock, a GaAs-based calculator[4], a GaAs-based floating-point adder/subtractor[5] and a GaAs-based mini central processing unit. They also carried out modeling of crosstalk among the high-density VLSI interconnections[6] and experimental measurements of propagation delays (of the order of a few hundred picoseconds) in the high-speed GaAs-based integrated circuits. In addition, a student studied the emergence of the Silicon-on-Insulator (SOI) technology[7,8] in the integrated circuit arena while another student compared the GaAs logic families with the transistor-transistor logic (TTL), emitter coupled logic (ECL) and complementary metal oxide semiconductor (CMOS) logic families by testing, analysis and benchmarking of a 74S381 ALU using MAGIC and SPICE. Brief outlines of the undergraduate projects carried out by the women REU students are given below:

3.1 Designing GaAs-Based Integrated Circuits Using L-Edit

IC design tool called L-Edit developed by Tanner Research is used primarily for designing Si

CMOS circuits. In this project, two REU students (SD, RM) extended its ability to designing GaAs-based ICs. The GaAs circuits designed were simulated by using S-Edit and the wave-form generator.

REU students Stephanie Draeger and Rebecca Morrison presenting their project results

3.2 Modeling of Crosstalk in the VLSI Interconnections

An REU student (LH) developed a program that can be used to study the crosstalk among the high-density interconnections on a VLSI chip. This program is based on the frequency domain modal analysis of two, three and four line systems. Two programs, one using C++ and the other using MATLAB were developed and used to analyze crosstalk for various values of the interconnection parameters.

3.3 Modeling of Electromigration-Induced Failure of the VLSI Interconnections

An REU student (JM) calculated the mean times to failure (MTF) of copper (Cu) and aluminum (Al) interconnections on the VLSI circuits using the perturbed hexagonal grain structure model. She realized that while Al has been a preferred material for metallic VLSI interconnects for a long time, Cu has been adopted recently by IBM and Motorola because of its lower resistivity and higher activation energy despite its disadvantages of lower temperature reactivity and diffusivity. This model can be used to analyze the dependence of MTF on current density, temperature and grain structural factors. It can also be used to study the electromigration-induced effects if Al-Cu alloys are employed as interconnect materials rather than pure aluminum.

3.4 Modeling of Very High-Frequency Effects in the VLSI Interconnections

An REU student (SW) studied the very high-frequency effects on the delays in the VLSI interconnections. She developed a transmission line model of single-level interconnect delays including such effects as the skin effect, conductor loss, dielectric loss and the parasitic capacitances which was used to study the dependence of delays on the various interconnect parameters.

3.5 Computer Simulation of GaAs and SOI Devices Using TCAD Tools

As device sizes shrink and new materials are added, it becomes more expensive, time-consuming and physically difficult to test each component and that device simulations using the TCAD tools is an economical alternative to experimental testing. REU students investigated the rapidly emerging Silicon-on-Insulator (SOI) technology for high-speed integrated circuits and concluded that SOI technology results in higher circuit speeds, lower power consumption and greater immunity to radiation-induced errors and is compatible with the existing IC fabrication processes. REU students (SB, AM) used the TCAD tools to simulate the performances of several GaAs- and SOI-based devices as functions of device dimensions and other fabrication parameters. They found out that the Silvaco Corporation's "Virtual Wafer Fab" (VWF) package consisting of process simulation software called ATHENA, device layout software called DevEdit, device simulation software called ATLAS and Tonyplot for displaying results could be used to simulate GaAs, SOI as well as conventional silicon devices. These simulations were designed to show both the efficacy of the materials and the simulation programs themselves. They explored the capabilities of these TCAD programs for several GaAs and SOI devices including short- and long-channel JFETs, digital GaAs E-MESFETs, HEMTs and SOI BJTs

.

REU student Sarah Bergstrom presenting her seminar

IV. Student Evaluations

At the end of each summer research experience, we surveyed the students as to their satisfaction with the program. Each year, students were very positive in their assessments of the program including their research experiences, interaction with other participants and faculty, and the effect the program had on their interest in pursuing graduate education and careers in semiconductor research. We also surveyed the students by e-mail in the spring. Their opinions of the program continued to be high. Almost all participants felt that this undergraduate research experience had greatly enhanced their overall education. Most of these REU students had accepted or were looking for industrial research positions or were planning to attend graduate schools.

V. Acknowledgments

This work is based on research supported by a grant from the National Science Foundation under Grant no. EEC-9619646. The support provided by the Michigan Technological University is also acknowledged. The authors like to thank graduate students Umesh Painaik, Kah-Jon Goo, Terrance Tan and Hua Ma for their help during this project.

Bibliography

1. Long, S.I., & Butner, S.E., *Gallium Arsenide Digital Integrated Circuit Design*, McGraw Hill, New York, 1993.
2. Goel, A.K., *High-Speed VLSI Interconnections*, Wiley Interscience, New York, 1994.
3. Goel, A.K., Sloan, M.E., Aytek, T., Bachhuber, S., Cadena, R., Damstra, F., Huynh, L., Jesiek, B., Kern, P., Lemmer, D., Lin, W., & Price, K., Research Experiences for Undergraduates in Design, Modeling and Measurements of GaAs-Based Very High-Speed Integrated Circuits, Proc. *ASEE North Central Section Spring Conf.*, Detroit, MI, pp. 54-58, 1998.
4. Goel, A.K., Lemmer, D., & Lin, W., A GaAs DCFL Implementation of a BCD Calculator: An REU Project," Proc. *14th Int. Conf. Computers and Their Applications*, Cancun, Mexico, April 7-9, 1999. (In Press)
5. Goel, A.K., Damstra, F., & Jesiek, B., Gallium Arsenide Based Floating Point Adder/Subtractor, Proc. *13th Int. Conf. Computers and Their Applications*, Honolulu, HI, pp. 348-351, 1998.
6. Goel, A.K., Huynh, L., & Jesiek, B., Computer Simulation of Crosstalk in the VLSI Interconnections: An REU Project, *Proc. 11th Int. Conf. Comp. Appl. Industry and Engineering*, Las Vegas, NV, 1998.
7. Lammers, D., SOI Enters Mainstream, *Electronic Engineering Times*, p. 30, January 13, 1997.
8. Colinge, J.P., *Silicon-On-Insulator Technology: Materials to VLSI*, Kluwer Academic Publishers, 1995.
9. Goel, A.K., Peacock, D.J., & Barber, T.S., *Designing GaAs Circuits Using MAGIC -User Manual*, Michigan Technological University.

ASHOK GOEL
Ashok Goel received his Ph.D. degree from The Johns Hopkins University in 1987. Currently, he is an Associate Professor of Electrical Engineering at Michigan Technological University. He is the author of a book "High-Speed VLSI Interconnections" published by Wiley Interscience in 1994. His research interests include modeling of interconnections and devices on the GaAs-based integrated circuits. He is a senior member of the IEEE.

MARTHA SLOAN
Martha Sloan received her Ph.D. degree from Stanford University and is a Professor of Electrical Engineering at Michigan Technological University. Her research interests are in logic design, computer networks and computer security. She is the author of three books and is a Fellow of IEEE, ACM and SWE.

SARAH BERGSTROM
Sarah Bergstrom is working on her BSE degree in Engineering with an honors minor in Classical Greek at Swarthmore College, Pennsylvania. She is a member of SWE and Tau Beta Pi.

ALELI MOJICA-CAMPBELL
Aleli Mojica-Campbell worked on her BS degree in Electrical Engineering at The University of Texas at El

Paso. She is interested in semiconductor design, DSP and fiber optics. She has served as the vice-president of Eta Kappa Nu, is a member of the Electrical Engineering Honor Society and is serving as secretary of the IEEE.

STEPHANIE DRAEGER
Stephanie Draeger is working on her BSEE degree in Electrical Engineering at the Michigan State University at East Lansing, Michigan. Her interests include embedded system design, optics and fabrication.

LEHANG HUYNH
Lehang Huynh received her BS degree in Electrical Engineering from the Michigan Technological University at Houghton, Michigan.

JAMI METEER
Jami Meteer worked on her BS degree in Electrical Engineering at the University of Notre Dame. Her interests include electronic devices and materials.

REBECCA MORRISON
Rebecca Morrison is working on her BS degree in Electrical Engineering at the Rutgers University at Piscataway, New Jersey. She is a member of IEEE, Tau Beta Pi and Eta Kappa Nu.

STEPHANIE WEITMEYER
Stephanie Weitmeyer is working on her BS degree in Electrical Engineering at the Calvin College at Grand Rapids, Michigan. She is a member and officer of Calvin's student chapter of the IEEE.