Research Experiences for Undergraduates in Design, Modeling and Simulation of GaAs-Based High-Speed Integrated Circuits

Ashok Goel, Martha Sloan, Sarah Bergstrom, Mikir Bodalia, Aleli Mojica-Campbell, Contessa DuBois, Martins Innus, Ying Lu, Jami Meteer, Steven Palmer, Nicolai Ramler, Vincent Singh

Department of Electrical Engineering
Michigan Technological University

Abstract

In this paper, the research projects carried out by the ten undergraduate students selected for the NSF funded undergraduate summer research site established at the department of Electrical Engineering at Michigan Technological University in the areas of design, modeling and simulation of GaAs-based very high-speed integrated circuits are outlined.

I. Introduction

Active research experience is one of the most effective techniques for training and motivating undergraduate students for careers in science and engineering. National Science Foundation recognizes this and supports undergraduate research under two programs: a) Under their "REU Supplements" program, NSF encourages principal investigators of NSF-funded research grants to include one or two undergraduate students in their existing projects; b) Under their "REU Site" program, NSF provides funds to set up undergraduate research sites consisting of nearly ten students to work on state-of-the-art research projects under the supervision of a faculty member.

Continuous advances in integrated circuit technology have resulted in smaller transistor dimensions, larger chip sizes and increased complexity. There is an increasing demand for circuits with higher speeds and higher component densities. Because of its semi-insulating property and the fact that the mobility of electrons is an order of magnitude higher in Gallium Arsenide (GaAs) substrate than in the widely used Silicon substrate, GaAs has emerged as a preferred substrate for the development of very high-speed integrated circuits. In fact, during the last few years, GaAs technology has emerged rapidly from basic research to device and circuit development. In addition, growth of GaAs on silicon (Si) substrate has met with a great deal of interest because of its potential applications in the new hybrid technologies. GaAs-on-Si unites the high speed and optoelectronic capability of GaAs circuits with the low material cost and superior mechanical properties of the Si substrate. The heat sinking of such devices is better since the thermal conductivity of Si is three times more than that of GaAs. This technology is expanding rapidly from material research to device and circuit development. Functional GaAs SRAMs of up to 1K in complexity have been demonstrated on Si sub-

strate. LED modulation rates up to 27 Mbit/s have been demonstrated on monolithically integrated GaAs/AlGaAs LEDs and Si MOSFETs. Further, it may be recalled that CRAY-4 supercomputer is based primarily on the GaAs-based high-speed circuits. In this paper, an undergraduate research site on GaAs-based high-speed circuits set up at the Michigan Technological University is described and the research projects carried out by the undergraduate students are summarized.

II. Undergraduate Research Site

During summer 1998, funded by a three-year grant from the National Science Foundation, an undergraduate research site was established for the second year at the department of Electrical Engineering at Michigan Technological University in the area of GaAs based very high-speed integrated circuits. This site consisted of ten undergraduate students selected on a competitive basis from institutions all over the USA. Eligibility criteria were: a) citizenship or permanent resident of the United States; b) completion of at least two years in electrical engineering, computer engineering or a related field with a grade point average of 3.0 or over. Major objectives of the REU site were: a) enhancement of student experience, competence, confidence and self esteem by working on a state-of-the-art electrical engineering research project; b) encouragement of students to pursue graduate studies in electrical engineering and to choose a career in microelectronics/VLSI research; c) improvement of student oral and written skills through written report and formal presentations.

In addition to the host institution, students were selected from University of Notre Dame, State University of New York at Buffalo, University of Texas at El Paso, Swarthmore College, University of Florida, University of Illinois at Urbana-Champaign and Rice University. Undergraduate students worked with electrical engineering graduate students and faculty members for ten weeks, from June 9 to August 15, on projects ranging from designing[1] a GaAs-based central processing unit to modeling the electromigration-induced failure effects in the high-speed VLSI interconnections[2] to computer simulations of GaAs- and SOI-based devices and circuits using the technological computer-aided design (TCAD) tools. Faculty interaction was maximum during the first few weeks and decreased as students became more and more independent in carrying out their projects. During the last week of the REU site, students submitted formal detailed written reports and presented formal seminars on their projects.

III. Undergraduate Projects

During summer 1997, the first year of the three-year project, the ten undergraduate students selected for this REU site worked with electrical engineering graduate students and faculty members for ten weeks on projects[3] ranging from designing a GaAs-based digital clock, a GaAs-based calculator[4], a GaAs-based floating-point adder/subtractor[5] to modeling the crosstalk among VLSI interconnections[6] to experimental measurements of propagation delays (of the order of a few hundred picoseconds) in the high-speed GaAs-based integrated circuits. In addition, a student studied the emergence of the Silicon-on-Insulator (SOI) technology[7,8] in the integrated circuit arena while another student compared the GaAs logic

families with the transistor-transistor logic (TTL), emitter coupled logic (ECL) and complementary metal oxide semiconductor (CMOS) logic families by testing, analysis and benchmarking of a 74S381 ALU using MAGIC and SPICE.

The ten undergraduate students selected for the 1998 REU site worked with electrical engineering graduate students and faculty members for ten weeks on projects ranging from designing a GaAs-based mini central processing unit (CPU) to computer simulation of GaAs and SOI devices using TCAD tools to the modeling of electromigration-induced failure effects in the VLSI interconnections. Brief outlines of these projects are given below:

3.1 Designing a GaAs-Based Mini Central Processing Unit

During summer 1997, realizing the inherent advantages of the GaAs technology, REU students designed several GaAs-based circuits including floating point adder/subtractor[5], high-speed digital clock and a GaAs-based calculator[4]. This year, four students (YL, SP, NR, VS) took up the challenging task of designing a GaAs-based mini central processing unit (CPU). They realized that, while for the past few decades, silicon-based technologies have been used to fabricate CPUs but the limits of silicon are being reached as the end of the millennium approaches and new materials must be investigated to continue the aggressive growth demanded by consumers and modern industry. They found that GaAs is considered a prime candidate for designing components with high speed and modest power consumption due to its high electron mobility, high switching speed, low capacitances and high packing density. Therefore, to illustrate and test the feasibility of GaAs-based components, they designed a GaAs-based mini CPU using the CAD tool called MAGIC[9] in conjunction with the GaAs technology files created by Long and Butner[1]. This CPU is based on a pipelined five-stage model using forwarding and branch detection to eliminate data and branching hazards. The five stages are instruction fetch, instruction decode, execute, memory and write-back stages.

3.2 Computer Simulation of GaAs and SOI Devices Using TCAD Tools

During summer 1997, an REU student investigated the rapidly emerging Silicon-on-Insulator (SOI) technology for high-speed integrated circuits and concluded that SOI technology results in higher circuit speeds, lower power consumption and greater immunity to radiation-induced errors and is compatible with the existing IC fabrication processes. This year, four students (SB, MB, AM, MI) realized that, as device sizes shrink and new materials are added, it becomes more expensive, time-consuming and physically difficult to test each component and that device simulations using the semiconductor technological computer aided design (TCAD) tools is an economical alternative to experimental testing saving large amounts of time, money and other resources. They worked on a project whose goal was to use the TCAD tools to simulate the performances of several GaAs- and SOI-based devices and to compare them with the corresponding silicon-based devices. They realized that while silicon is still the cheapest and most widely available material for integrated circuits (ICs), several products including many high-frequency low-power communication devices are possible only by using the newer more expensive materials such as SOI and III-V semiconductors, especially GaAs. They found out that the Silvaco Corporation's “Virtual Wafer Fab” (VWF) package

consisting of process simulation software called ATHENA, device layout software called DevEdit, device simulation software called ATLAS and Tonyplot for displaying results could be used to simulate GaAs, SOI as well as conventional silicon devices. They explored the capabilities of these TCAD programs for five different GaAs and SOI devices including short- and long-channel JFETs, digital GaAs E-MESFETs, HEMTs and SOI BJTs. These simulations were designed to show both the efficacy of the materials and the simulation programs themselves.

3.3 Modeling of Electromigration-Induced Failure in the VLSI Interconnections

In this project, two students (JM, CD) calculated the mean times to failure (MTF) in copper (Cu) and aluminum (Al) interconnections on the VLSI circuits using the perturbed hexagonal grain structure model. They realized that while Al has been a preferred material for metallic VLSI interconnects for a long time, Cu has been adopted recently by IBM and Motorola because of its lower resistivity and higher activation energy despite its disadvantages of lower temperature reactivity and diffusivity. Their model can be used to analyze the dependence of MTF on current density, temperature and grain structural factors. It can also be used to study the electromigration-induced effects of using Al-Cu alloys.

IV. Student Evaluations

At the end of each summer research experience, we surveyed the students as to their satisfaction with the program. Both years students were very positive in their assessments of the program including their research experiences, interaction with other participants and faculty, and the effect the program had had on their interest in pursuing graduate education and careers in research. We also surveyed the students by e-mail in the spring after the first year program (and plan to do so again this spring for the second year participants). Their opinions of the program continued to be high. Almost all participating students felt that this undergraduate research experience had greatly enhanced their overall education. Most participants had accepted or were looking for industrial research positions or were planning to attend graduate schools.

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ASHOK GOEL
Ashok Goel received his Ph.D. degree from The Johns Hopkins University in 1987. Currently, he is an Associate Professor of Electrical Engineering at Michigan Technological University. He is the author of a book "High-Speed VLSI Interconnections" published by Wiley Interscience in 1994. His research interests include modeling and simulation of interconnections and devices on the GaAs-based high-speed integrated circuits. He is a senior member of the IEEE.

MARTHA SLOAN
Martha Sloan received her Ph.D. degree from Stanford University and is a Professor of Electrical Engineering at Michigan Technological University. Her research interests are in logic design, computer networks and computer security. She is the author of three books and is a Fellow of IEEE, ACM and SWE.

SARAH BERGSTROM
Sarah Bergstrom is working on her BSE degree in Engineering with an honors minor in Classical Greek at Swarthmore College, Pennsylvania. She is a member of SWE and Tau Beta Pi. She is interested in control systems as they relate to both electrical and mechanical systems.

MIKIR BODALIA
Mikir Bodalia is working on his BS degree in Electrical Engineering at the University of Illinois at Urbana-Champaign with options in communications and control systems. He is a member of Phi Eta Sigma.

ALELI MOJICA-CAMPBELL
Aleli Mojica-Campbell is working on her BS degree in Electrical Engineering at The University of Texas at El Paso. She is interested in semiconductor design, VLSI and fiber optics. She is the vice-president of Eta Kappa Nu Electrical Engineering Honor Society and a member of the IEEE.

CONTESSA DUBOIS
Contessa DuBois is working on her BS degree in Electrical Engineeringwith concentration in computer engineering at Michigan Technological University. She is a student member of the IEEE and is actively involved in SWE. Her technical areas of interest are VLSI design and DSP.

MARTINS INNUS
Martins Innus is working on his BS degree in Electrical Engineering/Computer Science at the State University of New York at Buffalo.

YING LU
Ying Lu is working on his BS degree in Electrical Engineering/Computer Science at the University of Florida.

JAMI METEER
Jami Meteer is working on her BS degree in Electrical Engineering at the University of Notre Dame. Her interests include electronic devices and materials.

STEVE PALMER
Steve Palmer is working on his BS degree in Electrical Engineering at Michigan Technological University. He is interested in control systems and electronics. He is a member of the IEEE.

NICOLAI RAMLER
Nicolai Ramler is working on his BS degree in Electrical Engineering with options in controls and electronics at Michigan Technological University. He is a member of the IEEE.

VINCENT SINGH
Vincent Singh is working on his BS degree in Electrical & Computer Engineering as well as a BA degree in Mathamatical & Economic Analysis at Rice University in Houston, Texas.