Teaching Nano-Fabrication Materials Processing to Non-materials Majors

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Abstract

A new course under development that is designed to provide a broad understanding of the opportunities and limitations imposed by the processing of materials and structures in the micrometer to the nanometer regime is introduced. The historic focal point of micro-fabrication courses in engineering colleges has been electronic device manufacture. Accordingly, electrical engineering faculty typically teach this material and the course topics revolve around the construction of predominately silicon-based resistors, diodes, capacitors, metal oxide semiconductor field effect transistors (MOSFETS), and bipolar junction transistors (BJTs).

The advent of a myriad of new applications in recent years, in many cases not involving electronic materials, suggests that a new paradigm be developed for this instruction. Gene-chips, micro-electromechanical systems, micro-fluidic devices, micro-photonic devices, ink jet and aerodynamic disc read/write heads are just a few examples. These innovations were enabled and derived from fundamental unit materials processes that were originally developed to fabricate electronic devices. This new course aims to develop students' materials process skills and knowledge. We intend to enroll students from the entire science and engineering university community so that they may be prepared to contribute to the many exciting nanometer materials and systems discoveries that are possible as they pursue their careers.

There are many challenges to the success of this endeavor. Principle among these deals with the issues to be addressed if a hands-on laboratory instruction component is to be integral to the course. The resources needed for such instruction, in for example thin-film material deposition, can be significant. We discuss the approach of applying a graphical icon or "visual programming" to the development of process flows or sequences along with the interdisciplinary instructional format applied to an audience with the diversity level anticipated in this course.

Introduction

A new educational paradigm is needed to develop a skilled workforce capable of designing and building future generations of nanometer-sized electronic and physical structures. This paradigm must also encourage students to think outside of the proverbial "box". In this case the "box" is represented by the traditional approaches to nano-structure design and construction. The capabilities that have been handed to tomorrow's professionals through the efforts of technologists over the past four decades are significant and reinforce the need for a renewed "out of the box" perspective.

Approximately 40 years ago, Richard Feynman's address to the American Physical Society concerning “the problem of manipulating and controlling things on a small scale set a focus for the initial "out of the box" thinking effort. In his talk, “There’s Plenty of Room at the Bottom,” Professor Feynman challenged those present to develop an electron microscope with 100 times the resolution of the then current models to explore for example the arrangements of biological structures and molecular systems.

Professor Feynman continued to discuss the manufacture of scaled, tiny, items and the manipulation of materials on an atomic level. He proposed that small items would have little weight and therefore inertia should not be an issue and that small items should be much stronger. He further noted that structures might of necessity be fabricated from amorphous assemblies of atoms, since grain structures of materials would cause a coarse or rough surface. Problems with material resistance and items sticking together by Van der Waals forces that for items of small size scale would be stronger than the force of gravity on the small parts were also noted. In retrospect, initial "out of the box" thinking has brought much of what Professor Feynman postulated in that seminal lecture to pass in the intervening forty years and yet there is much more to accomplish.

Semiconductor device technology has advanced steadily from the 1947 invention of the point contact transistor by Bardeen, Brattain and Shockley at Bell Telephone Laboratories. Gordon Moore, a founder of Intel, on the occasion of his retirement to the company board noted that a component density of a billion transistors, or “bits” representing a logical 0 or 1, per chip was close at hand. He postulated that at this high density the traditional business model used to price components by a cost per bit would need to be re-thought. Computing capability provided by such devices could enable voice recognition and other as-yet undeveloped innovations. Even so, the minimum feature size of transistors in a billion-transistor chip will be on the order of 100 nanometers. By comparison a significant globular protein molecule such as an enzyme is roughly one-fifth this size. Moore's Law of device scaling predicts that the number of transistors on a chip will double every two years. Following this law, electronic devices will soon reach physical limits. For example, dynamic random access memories use stored electrons to define a binary logic state of one bit. For a high capacity memory cell, 250,000 electrons represent the quantity of stored charge per bit. Using a Moore’s Law extrapolation, this quantity of charge will drop nearly to the physical limit of one charged entity, an electron, per bit within thirteen years. None the less over the intervening decades following the introduction of Moore’s Law, technology has seen the advent of personal computers, hand held electronic devices including calculators, beepers, phones, global positioning devices, and many other innovations. In the industrialized world, one finds that the number of chips that are encountered daily by individuals is steadily increasing.

The evolution from the construction of a single "gigantic" transistor at Bell Labs in 1947 to today's automated manufacture of a suite of microelectronic devices has followed a linear progression in the development of design and processing skills. These skills will continue to service the semiconductor processing industry. However, additional challenges, as Feynman envisioned, prevent sole reliance on this set of skills alone.

Micro-electromechanical systems, MEMS[1], are millimeter to micrometer-sized assemblies of gears, mirrors, tiny channels, heaters, ink jets, and other tiny structures such as aerodynamic read/write heads for memory discs. MEMS systems include complex pick-proof or secure locks, miniature chemical separation columns, display devices such as Texas Instrument's DLP chips, GeneChips that help assay DNA, and tiny cell manipulators to list but a few. The development of the scanning tunneling microscope and the subsequent introduction of the atomic force microscope in the 80's and 90's are a further realization of Professor Feynman's challenge. These two metrology systems enable the characterization and manipulation or both single atoms and molecules. The discovery of fullerene molecules and an elongated variant of them, carbon nanotubes, are further enhancing our ability to manipulate and measure nanostructures and atoms. Professor Charles Lieber and his team at Harvard University recently demonstrated a nano-circuit fabricated from nano-wires that were placed using MEMS-type micro-channels[2].

The innovation successes reviewed above initially required the application of engineering practice beyond the set of materials design and process procedures known in the art at the time of their inception. However, at this point these materials processing unit operations are routinely applied to the fabrication of electronic devices. Integrated circuit engineering curricula for this reason have been centralized in Electrical Engineering departments. Prerequisites for IC courses include circuit fundamentals, semiconductor physics and analysis and design of simple device structures such as semiconductor diodes.

By contrast, IC processing factories "live or die" based on their material processing unit operations and innovations. These expensive factories are in the realm of chemical engineers and physicists with electrical engineers performing optimization of the interaction of process methods with device design and operation. A broader treatment of the materials methods and connecting details associated with the material process unit operations utilized to fabricate small structures is needed. This treatment combined with students from an expanded set of disciplines will allow a new generation of "out of the box" thinkers to better address the challenges that face the new material-processing world.

New Course Structure

The traditional course approach has been device centric, playing off classical semiconductor and circuit courses. Yet upon entrance into such an IC fabrication technology course, students have little knowledge or expectation of the actual structure of physical devices. To these students an IC component is intellectually tied to a circuit schematic symbol and physically associated with a packaged device such as a dual in-line package or DIP.

As part of the new course, students will learn silicon based unit material fabrication processes including: thermal oxidation, impurity incorporation and solid state diffusion, thin film deposition, lithography, etching, chemical processing, assembly and packaging. Process sequences are derived from a resource bin filled with such unit processes. Yet even the best students have difficulty with this approach. They have problems associating a final threedimensional structure with a specific sequence of processes. Another way of saying this is that students have difficulty developing a consistent processing philosophy, or understanding of when to select one process over another.

It is our contention that, if properly framed, materials-centered device and nano-fabrication technology courses could be opened to a broader audience than students from the engineering college alone. A minimal set of prerequisites might include first year calculus, chemistry, and perhaps introductory physics. Electronic devices covered would include a rather complete set: Resistors, capacitors, diodes, BJT's, MOSFETS, CMOS, compound semiconductor, optical, and quantum devices such as single electron transistors. Also devices derived from electronic device unit processes include MEMS structures. Topics of simulation, characterization, and process sequences will also be covered. Micro- and nano-structures including channels, heaters, mirror systems, nano-molecular systems, as well as physical structural elements integrated with electronics. Nanostructures including carbon nanotube probes, quantum devices, and nanowires should also be included.

To accomplish these goals the course under development includes the following topics:

Introduction—Device structures consistent with IC fabrication and extending into nanotechnology such as fluid, photonic, mechanical, nano-electrical, and molecular.

Material science—Physical and molecular parameters and how they change with the size and scales of structures. For example proceeding from macro to micro and then to nano, how parameters such as resistivity, friction, and force on an object change with size? When do you stop and abandon predictions set by a given parameter, or apply a corrective model? In the absence of a corrective model when do you look for another variable to use that might fit the situation better?

Parameters at semiconductor scales—Micron-sized applications such as appliances and sensors. How are appliances dependent on the data that a sensor provides? What are the interaction issues between the two entities?

Macro design—Identify/create applications for existing technologies. Design an electronic component and address the issues posed by scaling it to smaller and smaller dimensions.

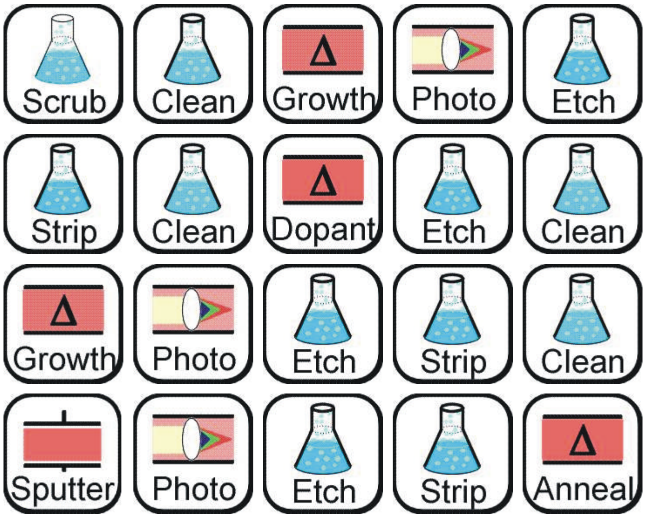
Design philosophy—Encourage "out of the box" thought. Sensors will be used as the model for this discussion. Sensors sense the physical universe via a front end using chemistry or physics such as stress, strain, or electromagnetics. At the rear end of sensor systems we again see physics but in the form of electronics—voltage, current, resistance, capacitance, light and color, sound, or interaction with humans.

Design Issues—Sensors couple the world through engineering science to humans. A major issue is timing. Sensors are equilibrium devices, we don't want to acquire and save values while the sensor is changing its mind. If data is taken too fast or slow the result is waste.

Device Construction—Materials processes or unit processes. How do the bulk structure, the thin films present, chemistry, and physics of the systems employed interact with or impact the structural design?

Process flows and integration—The philosophy of unit process selections. How do process sequences affect the final implementation? For example, the process flow in Figure 1 is represented by a sequence of graphical icons with each representing a specific unit process. When executed in series from the top left down through the figure row by row from left to right the final product is either a resistor or a diode. The icon representation provides a capability for students with a variety of backgrounds to develop sequences that all may understand. With reference to the figure, icons may be grouped in process families. For example each of the icons with a flask as part of the symbol are members of a chemical process family. The *Scrub*, *Clean*, *Strip*, and *Etch* processes all occur in a liquid chemical environment. The icons themselves may also each represent a series of unit processes.

Wafer level Process sequence



Product: Resistor or Diode

Figure 1. Process sequence that results in either a resistor or a diode.

Figure 2 depicts the Photo icon and notes the processes steps included within the step. Each of the process steps may have its' own recipes and procedures. These may vary depending upon the process application. The most difficult aspect of developing process sequences for students is determining which process from their toolbox to apply in a given situation. Therefore each icon should have implicit in its definition an indication when it could be applied just as a subroutine in a software program defines which variables are passed to it and those that it modifies as it performs its function. For this course, an augmented set of icons will need to be developed to address processes appropriate for the broader base of materials and dimensional scales that will be applied as the course moves toward processes at nanotechnology scales.

Included processes:
Apply adhesion promoter
Spin coat photoresist
Pre-exposure bake
Align and Expose resist
Develop photoresist
Post-develop bake
Metrology and Inspection

Figure 2. Photo icon and included process steps.

Hands-on Laboratory

The course lecture topics will be supplemented with hands-on laboratory experiences. Students may benefit in a number of ways from interaction with the tools and methods commonly used to fabricate structures. Typical instruction lab process tools are usually development-scale process tools. Such tools are easier to use than full-scale IC production tools and yet there is still a problem with them. New students are frequently not allowed to use even the development-scale apparatus due to their cost, complexity, and the hazards they pose to the student operators should their parameters be improperly set. An equipment philosophy that addresses these issues has recently become available on the commercial market. The tools offered by one company in particular[3] allow students to fabricate thin films, perform lithography, and carry out chemical processes in a generally safe and economical manner. This laboratory equipment enables students to perform experiments and execute designs based on a minimum geometry of roughly 50 micrometers with only minimal intervention by an instructor. The cost of a tool set capable of performing a majority of integrated circuit unit processes is roughly $250,000. This total is much less than the cost of a set of development-level equipment that could perform the same functions. This cost is however not insignificant and points to the economics of offering such a processing course. Clearly, however, the more students that could take advantage of such a laboratory experience the better.

Conclusions

The authors believe that processing courses as presently offered will eventually cease to meet the needs of future engineers and scientists. These courses are usually based on silicon and yet there are many other materials that can take advantage of a silicon process tool set. Most of the nanotechnology labs in the world today had some components of silicon processing in their near history. This course represents an initial effort to diverge from the current mindset and allow students to think “out of the box” as they translate Professor Feynman’s challenges into their careers.

References

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