The Integration of the Complex Programmable Logic Devices with the Introduction to Digital Logic Design Course

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Abstract

The field programmable logic devices (FPLDs), which include both field programmable gate arrays (FPGAs) and complex programmable logic devices (CPLDs), are modern technologies defining the new essential engineering skills. Although many commercial programmable device products for high education exist on market, they usually have multiple functionalities and they are expensive for many engineering students. In order to offer students more opportunities to use new technologies in the digital labs or at home, the author designed two low cost CPLD boards during the summer of 2004. The author taught computer engineering and electrical engineering students the art of the logic design using the FPLD technology at the California State University, Sacramento (CSUS). This paper describes the issues related to the integration of the CPLD boards with the Introduction to Digital Logic Design course.

Introduction

Introduction to Logic Design is a common engineering course that is offered at many universities. In the past, students studied digital logic circuits by designing the small size transistor–transistor logic (TTL) circuits[1] on the breadboards. It was time-consuming and troublesome to wire and modify such circuits. Fortunately, the new FPLD technology allows the designers to use the Hardware Description Language (HDL) to prototype the large size digital circuit quickly[2]. However, the commercial FPLD products on market are usually expensive. Although some major FPLD vendors such as Xilinx[3] and Altera[4] donated FPLD boards to universities, the engineering students in many universities had to share boards in the labs due to the limited number of available boards. This paper presents a solution to this problem by using small, and flexible CPLD boards in the Introduction to Digital Logical Design course at CSUS. These boards can be combined with the breadboards for students to design the simplest digital logic gates at the beginning of the class. The more complex designs such as the finite state machines, the simple microprocessors and so on can be implemented on the CPLD boards later in the class. These design activities can not only stimulate students' critical and creative thinking, but also extend their knowledge. This will help them enter upper level digital design classes to build more complex digital system[5]. The

author designed two low-cost CPLD boards to offer students an opportunity to afford CPLD boards and use them in the labs or at home.

CPLD Boards

The author designed two CPLD boards during the summer of 2004. Figure 1 is a picture of a 6" x 4.3" CPLD board. This board used the Altera EPM7128S chip. Another CPLD board with almost the same PCB layout used the Xilinx XC95108 chip.

The Altera EPM7128S CPLD is the second-generation MAX architecture EEPROM-based programmable logic device. It has built-in IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface with 5V in-system programmability. It has 8 logic array blocks, 128 macrocells and 2500 usable gates [6].

The Xilinx XC95108 CPLD is a high-performance device using the advanced CMOS 5V Fast FLASH™ technology. It supports in-system JTAG programming and test capabilities. It provides 108 macrocells with 2,400 usable gates. It has 3.3V or 5V I/O capability [7].

Figure 1. The CPLD board designed for the undergraduate logic design course

In Figure 1, there are thirty-four switches at the bottom of the CPLD board. The sixteen switches on the left are the general inputs to the CPLD chip. The two white switches in the middle are useful "hand clocks". Each push and release of the big white switch will generate one clock pulse after the debouncing circuit is implemented on the CPLD chip. The sixteen switches in four rows on the right are designed for the keypad applications. One oscillator and one seven-segment display are arranged on the left of the CPLD chip. One power jack and one JTAG downloading connector are designed on this board. The twenty LEDs on the

top indicate the input or output logic levels. In addition, a 34-pin connector on the top is available for the user to access the power, the ground, and many input/output (I/O) pins of the CPLD chip.

Classroom Integration

The CSUS digital lab provides every student with a parallel port connector, and a power supply adapter. The early assignments for students are to use breadboards to build simple logic circuits using AND, OR, NOT, NOR, NAND, XOR, and the other basic logic chips. Students use digital multimeters to make measurements and trace problems in the digital circuits. The 5V power supply on the CPLD board can be used to power the breadboard.

Although students can build small size adder and comparator circuits on the breadboard, it is not trivial for them to build large size logic circuits because of the complicated wiring. Instead of using breadboards, students learn how to use Verilog hardware description language to design large circuits quickly on the CPLD board.

First, students need to design SR latches in Verilog to debounce the switches. It is interesting for them to check the functions of SR latches by observing the relationship between the output LEDs and the input switches of the SR latch circuits on the CPLD boards.

Then students can build the edge triggered JK flip-flop in Figure 2 and implement this design using Verilog. They can use one white switch on the CPLD board as a hand clock. This will give them the understanding of the "edge trigger".

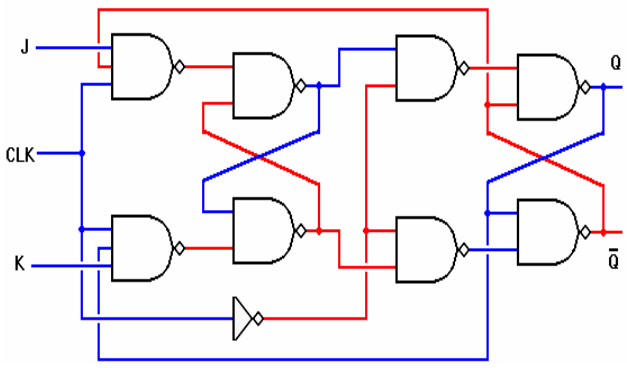


Figure 2. Edge triggered JK flip-flop

Furthermore, students can quickly build the large circuit system by using Verilog hierarchical design strategy. For example, they can use the JK Flip-Flops designed in Figure 2 as

components to build a 4-bit binary counter with parallel load.

Usually, the fun lab projects greatly fascinate students. Students are very excited to see some real world applications such as displaying the year and date in a serial shifting sequence on a seven-segment display.

Other general designs are the data transfer circuits, the serial/parallel shift register, the multiplexer, the encoder, the decoder, the finite state machine, the arithmetic logic unit, the simple microprocessor, and so on.

For some given circuits, students can compare the structural designs down to the basic gates with the behavioral description designs. While the structural designs help students understand the basic gate and register level structure of their designs, the behavioral description designs allow students to build the behavioral models for the large and complicated digital system, and speed up their design process.

Simulation and Hardware Implementation

A simulation study is crucial for students to understand the function of the circuits, minimize the design time, and verify the design results. After the successful simulation, students can implement their designs on the CPLD board. The whole design process is illustrated in Figure 3.

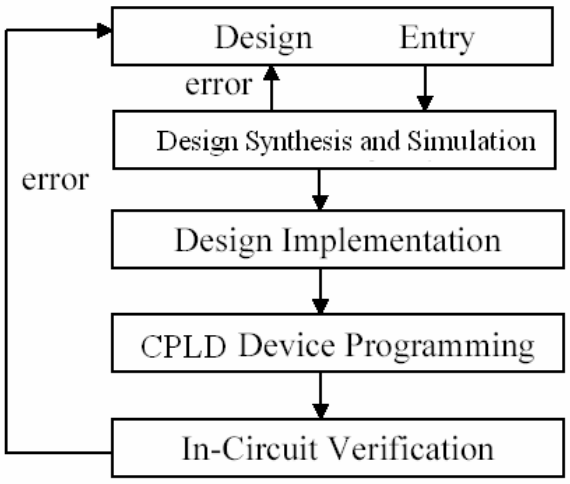
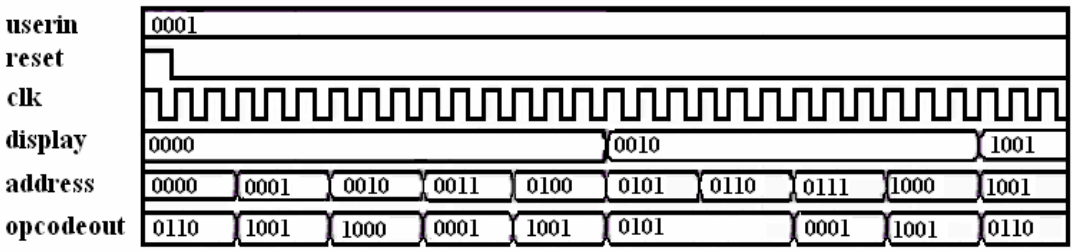


Figure 3. The CPLD digital circuit design flow

At the design entry stage, students can use either the schematics or the hardware description language. Then, they use the computer aided design tools to synthesize their designs and run simulations. If there are any errors, they need to go back to the design entry to modify their designs. After the successful simulation, they can implement their designs on the CPLD board. This usually goes through the translation and the mapping process. When the designs are downloaded on the CPLD board, the CPLD chip will be programmed and configured. The on-board hardware verification is the last step for students to check the design results. If there are any errors, students need to go back to the design entry and redo the whole design flow.

For a relative large digital system design, the sufficient display resources are usually welcome by students to do onboard hardware verification. Moreover, it is very beneficial for students to control the timing of the sequential circuits on the hardware, so that they can have time to check the results of each operation step.

For example, in a design of a simple microprocessor, the control and the data path of the microprocessor can be implemented on the CPLD board. Figure 4 shows the simple microprocessor design simulation results. Ten opcodes are simulated. The simulation waveform shows the values of opcode, address, userin data, clock cycles, and display. Students can add any other necessary signals into the simulation window to check the results. These results help students understand how opcodes and addresses function, as well as how clock cycles affect the CPU operation. Students are able to inspect the possible design problems by checking the simulation results.




```
0:        opcodeout<= clear;          //4'b0110
1:        opcodeout <= display;       //4'b1001
2:        opcodeout <= read;          //4'b1000
3:        opcodeout <= increment;     //4'b0001
4:        opcodeout <= display;       //4'b1001
5:        opcodeout <= left_rotate;   //4'b0101
6:        opcodeout <= left_rotate;   //4'b0101
7:        opcodeout <= increment;     //4'b0001
8:        opcodeout <= display;       //4'b1001
9:        opcodeout <= clear;         //4'b0110
```

Figure 4. The simple microprocessor design simulation results

The next step after the simulation is the hardware implementation. The CPLD board has twenty LEDs and one seven-segment display. Twenty LEDs are divided into five banks and two colors to give good visual appearance. One seven-segment display can be used to display any number or letter. Any one segment can also serve as a single display to indicate the logic level of the digital signal. The single oscillator on the CPLD board, which can generate the square clock wave, is good for any automatic sequential timing control. In addition, the white switches on the CPLD board can serve as the "hand clock" for the manual control of the sequential operation.

After students implement their simple microprocessor designs on the CPLD board, they can push one "hand clock" switch to control the timing of the simple microprocessor operation. They can observe the results on LEDs or on the seven-segment display after each clock cycle. They can use a reset switch to turn the microprocessor operation back to the beginning at any time. The "hand clock" allow students to have enough time to look at the displayed results, analyze their design operations, and ask the instructor questions.

Conclusion

Due to the widespread of field programmable logic device technology in the industry, the universities need to provide students opportunities to obtain the skills on using this new technology. Although high cost commercial CPLD or FPGA boards with multiple functionalities are one option for universities to equip their digital labs, this provides only limited access for most of the engineering students. The author of this paper designed two CPLD boards for the Introduction to Digital Logic Design class and lab. These boards can be used with breadboards to provide students with the flexible and powerful modern digital circuit design tools. These boards are cheap and students can buy them and use them in the digital labs or at home.

This paper discussed how the two CPLD boards could be integrated in the classroom. It presented the features of the two CPLD boards designed by the author and the advantage of using hardware description language in the introduction to digital design lab. It described the design flow of using programmable logic device technology. It pointed out the important simulation and hardware implementation issues.

Interacting with the flexible CPLD boards will increase the interest of students on the digital hardware design and attract students to attend the upper level digital design classes. Different experiments on CPLD boards can also be used to test students on their knowledge and give feedbacks to the instructors on how well students learn from the classroom lectures.

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Biographical Information

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