Session 2548

VHDL and Small Format Color Displays
"Video Images Make Learning Fun"

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Abstract

Rochester Institute of Technology requires a course in Principals of Design Automation for Electrical Engineering Technology and Computer Engineering Technology students. At the completion of the course, students are expected to know the basics of coding for synthesis, test bench techniques, modelsim simulator, and the Xilinx tool flow for targeting complex programmable logic devices (CPLD's) and field programmable gate arrays (FPGA's).

A quick survey of the typical college student showed that they love video images. It could be a video clip captured with a digital camera, a digital video playing on their laptop, or digital images captured with their camera phone. This paper reviews and discusses how an FPGA platform was selected and integrated with a QVGA(320x240) color display. It details how an eight lab sequence was developed to allow the students to accomplish a project goal of playing a video image sequence on the QVGA display. This paper also illustrates how additional ABET outcomes such as applied technical problem solving, technical writing, configuration management, team dynamics, communications, and ethics were integrated into the course content.

Introduction

Rochester Institute of Technology requires a course in Principals of Design Automation for Electrical Engineering Technology and Computer Engineering Technology students. At the completion of the course, students are expected to know the basics of coding for synthesis, test bench techniques, modelsim simulator, and the Xilinx tool flow for targeting complex programmable logic devices (CPLD's) and field programmable gate arrays (FPGA's). The prerequisites are Digital System Design and a formal, structured programming course.

Course Description

An advanced course in the VHSIC Hardware Descriptive Language (VHDL). The course provides an in-depth coverage of the language and describes the VHDL design environments that will be used for synthesis and verification. Topics include the behavioral, dataflow, and structural modeling of both combinatorial and sequential logic, design methodologies, synthesis and optimization. An IEEE-1076 standard VHDL development system will be extensively utilized to synthesis VHDL for PLD, CPLD and FPGA applications. The prerequisites are Digital System Design and a formal, structured programming course. Class 3, Lab 2, Credit

Rationale & Goal

Upon success completion of the course, the student should be able to design VHDL models using behavioral, data-flow, and structural design methodologies. Design, code, and synthesize into programmable logic devices (PLD, CPLD, FPGA) both combinational and sequential logic with VHDL. Understand the differences between VHDL modeling for simulation and logic synthesis. Use VHDL to model hierarchical designs with standard and generic component instantiation. Apply Global Constraints to communicate performance objectives. Use the Report files to analyze implementation results. These are specific ABET outcomes which are measured for the course.

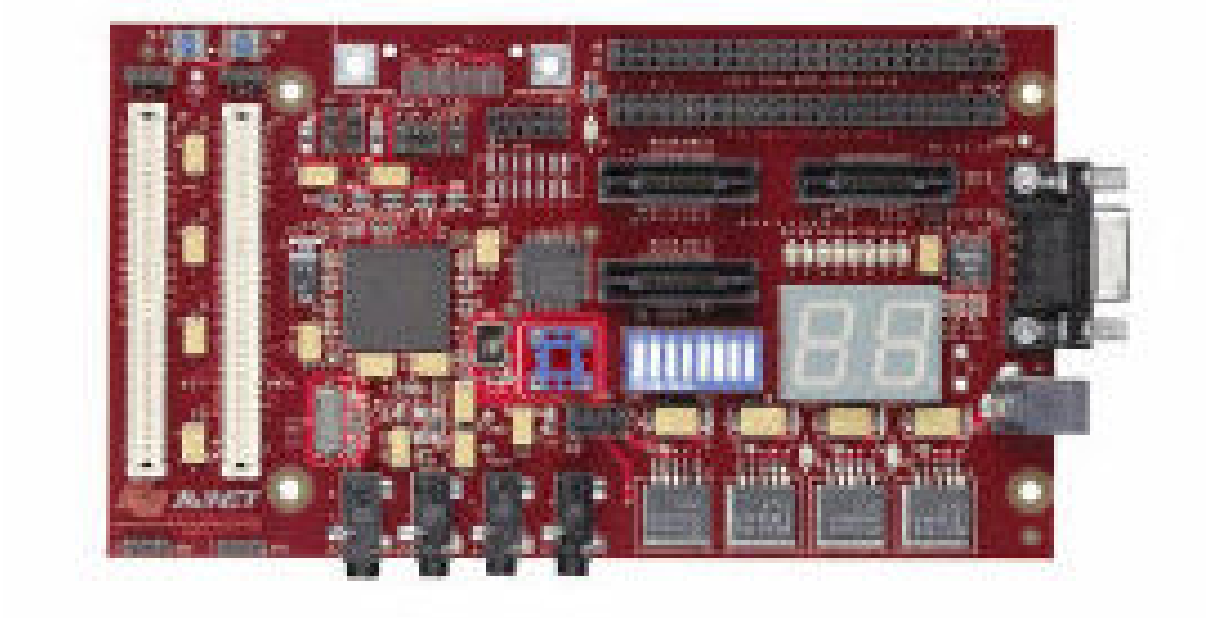
Laboratory Platform Development

Approximately three years ago the lab was taught using the Xilinx 9536 Complex Programmable Logic Device(CPLD). To enhance the educational value for the student an 8 lab sequence that culminates with the completion of a project was developed. Each lab develops one important module of the overall project. The final lab would integrates each module into a complete system for final verification and validation.

To implement the display project and expose the student to leading edge technology, a new platform was selected. Over the summer of 2003 many FPGA platforms were analyzed and the Avnet Spartan IIE XC2S200E platform was selected as shown in Figure 1.(1) The board was designed by Avnets Design Services division.

The second part of the platform development was to integrate a color display with the FPGA platform. The goal was to expose students to a quarter VGA TFT display, used in many cell phones and PDA applications.

Figure 1: Spartan IIE FPGA platform



The platform was selected because it was the most flexible platform available at the time. It has four 50 pin headers which allow for different porch boards to be designed. The features of the board are described below.

Features

It has a Xilinx Serial EEProm (XC18V02VQ44C) which is used to store the xilinx configuration file. The field programmable gate array is the Xilinx Spartan-IIE XC2S200E-6FT256C.
The Board IO Connectors are:

- Two 50-pin, 0.1 expansion connectors
- Pads for 3 mictor connectors
- Pads for two 140 pin general purpose IO
- Pads for 26 pin MDR connector for LVDS

The power available on the board is flexible. (+5, +3.3, +2.5, +1.8, +1.5 Vdc) There is an audio codec (TI ALV320C23 16 bit audio codec) mounted on the bottom of the board. Communication is via the RS232 port (DB9). To configure the board a JTAG header is provided. There are also some miscellaneous features, 8 dip switches, dual 7 segment display, 8 leds, 2 pushbutton switches, 50 Mhz oscillator and an additional oscillator socket.(1)

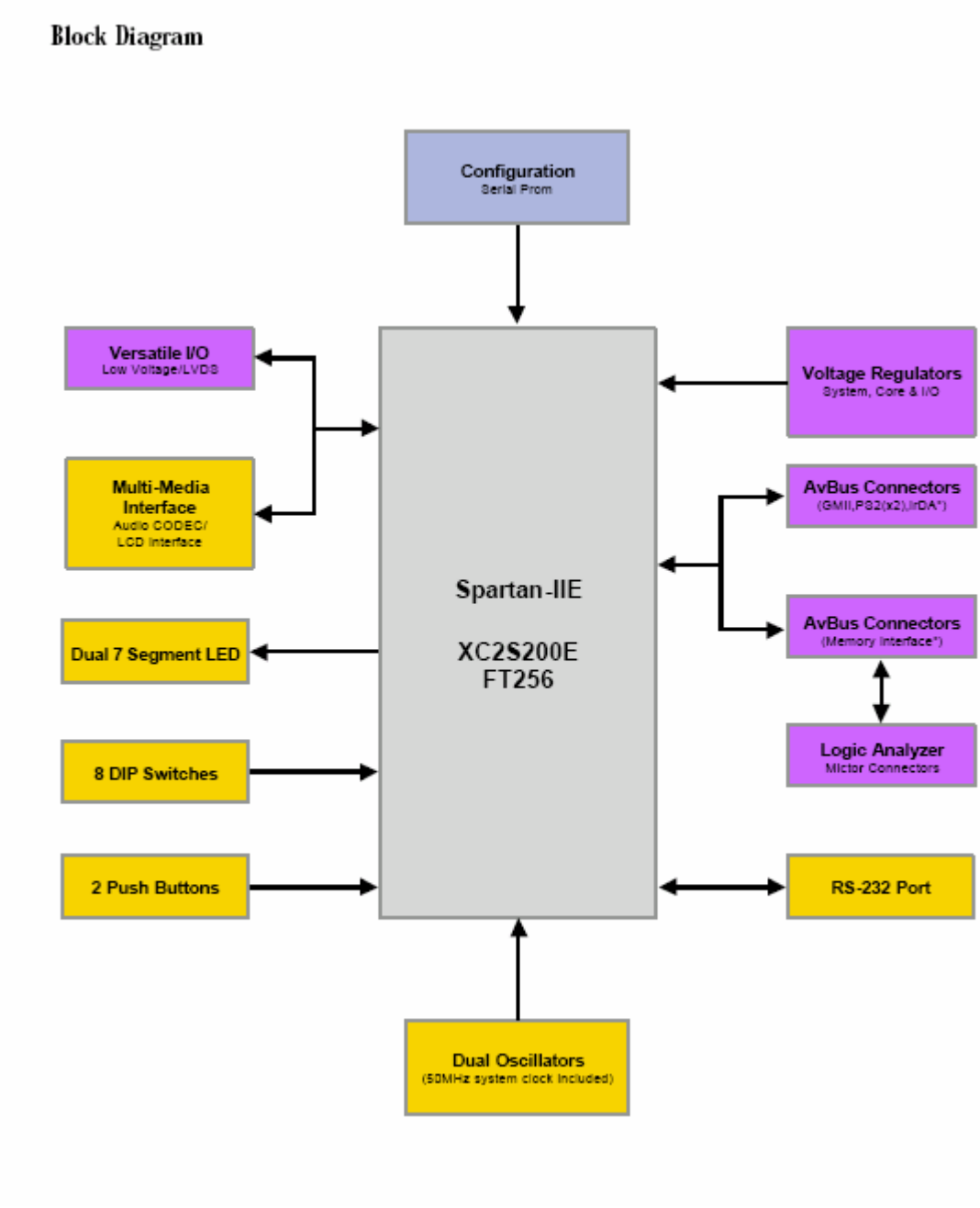


Figure 2: Block Diagram

The block diagram shown in figure 2, highlights the major components and features on the FPGA board.(1) The block diagram makes it easier to visualize the major board features. Students who had been on a co-op recognized the importance of learning the new platform.

Quarter VGA display
The Sharp QVGA(320x240) TFT display was selected.

SHARP	**LQ057Q3DC02**	**5.7IN TFT 320X240 - 6 BIT DIGITAL INPUT**
ENDICOTT	**8M052322**	**INVERTER**
ENDICOTT	**H0103305**	**12" INVERTER POWER CABLE**
QUADRANGLE	**QD3577**	**DATA CABLE FOR SHARP DISPLAY**

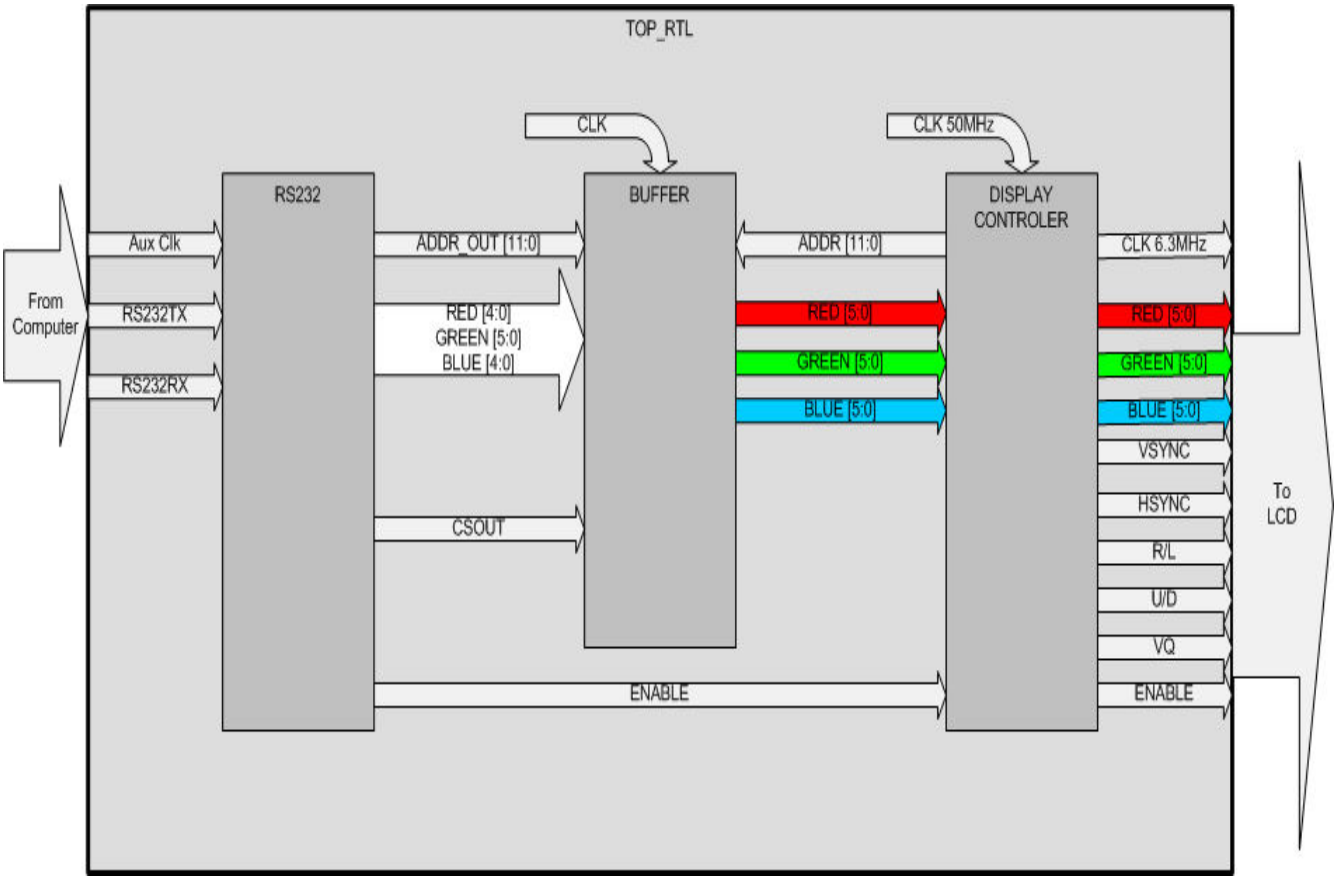
It is a 5.7 inch color display. The display was mounted and packaged in plexi-glass to protect both the student and the display during testing. The enclosure also discourages the student from changing the connector pin out during debug.

Lab Sequence

Eight labs were developed that culminate with the completion of a display project. Each lab implements one important piece of the overall display project. The final lab integrates and tests the complete display system.

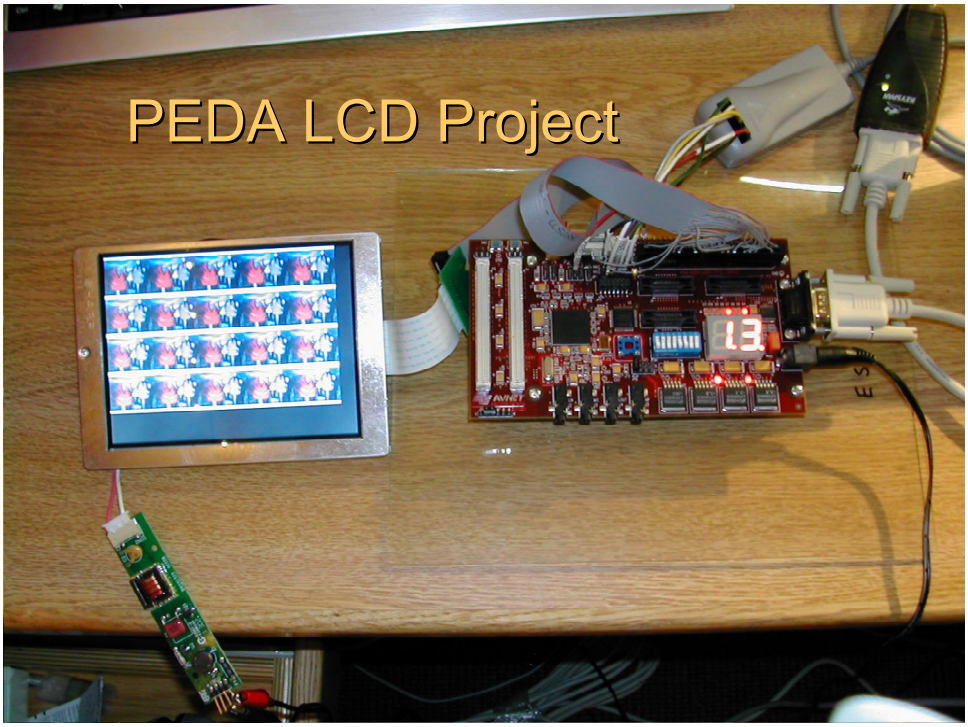
To test the feasibility of the concept, a group of four students performed an independent study for five weeks. The students were provided with the Spartan IIE board, the Sharp QVGA, and the associated laboratory documentation. Their goal was to display interesting images and patterns to the display, using the RS232 port for control. The group and I met weekly to discuss problems and issues with the design. The top-level Diagram shown in figure 3 was reviewed with the group.

Figure 3: Toplevel Diagram



The group quickly came up to speed on the technologies. They were able to implement and present their project to the rest of the class during week 11. The project was a success. The students were excited and worked many more hours than normally required to receive an A in the course. A picture of the working student project displaying a repeated image sequence is shown in figure 4.

Figure 4: Image of the working project



Lab Steps

The following steps are followed and documented for each laboratory.

1) Analysis
2) Design
3) RTL Coding
4) Test-bench Coding
5) Verification
6) Validation
7) Lab report write up

Topics covered and reinforced each Lab

1) Coding Guidelines – The coding guidelines for both Digital System design and Principals of Electronic Design Automation are reviewed with the students at the beginning of the quarter. All labs are graded based on the coding guidelines.
2) Code Reviews – Students are chosen at random to perform a code review on a module they have designed. The review lasts approximately fifteen minutes. Students learn different techniques by reviewing code different from there own. In addition live examples are presented which highlight both good and bad coding technique.

3) Project Presentations: Students that develop a novel technique while designing the project are selected to present their project to the class. Two examples from previous classes include a flying bird in a repeating sequence and a Perl interface running on a laptop that allowed the selection of different visual images.

Laboratory Sequence and Descriptions

Students are allowed to work individually or in groups of 2. If a student decides to work with a partner they must decide at the beginning of the quarter. Switching of partners is not allowed. Also, if the student works with a partner they are each responsible for 50% of the project.

Lab 1 **Hello World**: This lab provides an introduction to the Spartan IIE board. The task uses switches as inputs to control LED's as described by the lab. The student learns how to map signals to the appropriate pins on the xilinx board by utilizing a User constraints file(UCF). The clock frequency is also specified in the UCF file.The reports generated from synthesis are analyzed carefully.

Lab 2 **Serial port**: The lab requires the students to implement the receive side only for the serial port. If the student also implements the transmit side, it was counted as bonus points. The basics of the x-terminal interface are also reviewed.

Lab 3 **Registers and address map**: Using the serial port students write to a defined set of registers. The basic understanding of address mapping and multiplex structures for reading registers was covered.

Lab 4 **Delay Lock loops**: This lab focuses on the clocking and reset requirements for the project. It discusses why global clock lines are important to minimize clock skew. It also covers, in detail, the use of a Xilinx delay lock loop. This was the foundation of the clocking and reset architecture the student will use for the remainder of the project.

Lab 5 **Basics of Synchronous Ram**: Xilinx FPGA's have internal Ram which can be a valuable resource if utilized properly. In this lab the student learns about synchronous static ram. The student learns how to instantiate and use the Xilinx synchronous static ram in the design. The reports are carefully analyzed after synthesis to view the effect utilizing ram has on the available FPGA resources.

Lab 6 **Image Transfer or Pattern Generation**: To keep the project manageable the pattern or image sequence sent to the display was left up to the student. This allows the student to make tradeoffs between image size and the available memory and logic resources on the Xilinx FPGA.

Lab 7 **Color Displays**: Color displays and the basics of Thin Film Transistor(TFT) display technology was discussed. Specifically the digital video timing sequence necessary for the display controller was discussed in detail. The student quickly learns in this lab how a 3rd party data sheet can be misleading and difficult to interpret.

Lab 8 **Project Integration**: Project integration was taking place each lab. The student was instructed to continue building on their design and verification environment. The students that maintain a clean design and verification environment proceed through the final verification and testing phase quickly. This lab is the culmination of ten weeks of effort that completes the display system.

Student to Student Learning

The purpose of the laboratory assignments in the course was for students to learn more about digital system design and modeling than can be covered in the course lectures and readings. Learning and knowledge retention occur while working on the projects. The labs are learning exercises, not tests. Therefore, students are encouraged to talk with other students about approaches to solving the assigned labs. However, all design and development was to be done individually. All VHDL programming and the associated lab reports must be individually developed. It was stressed that copying work from other students will result in all involved students receiving a grade of 0 for the assignment and the possibility of a failing grade in the course. This effectively covers an ABET outcome which teaches ethics.

The syllabus contains the following warning.

"Plagiarism" (from a Latin word for "kidnapper") is the presentation of someone else's ideas or words as your own. Whether deliberate or accidental, plagiarism is a serious and often punishable offense. Deliberate plagiarism includes copying a computer code from a source and passing it off as your own or handing in as your own work a program you have bought, had a friend write, or copied from another student or a published source.

Each RIT student is expected to maintain high standards of honesty and ethical behavior. All individual assignments must be completed individually. Therefore, it is required that you add these comments at the top of each program you submit for course credit.

```
//--------------------------------------------------------------------------------
//      On My Honor……
//      I have not copied program code from others or from published sources.
//      The code for this assignment was created by me and is original.
//--------------------------------------------------------------------------------
```

Grades and Evaluating Student Learning

The class was developed for delivery in a one quarter, 11 week format. The course was developed with a focus on lab work. The best way to improve design skills is to practice with a mentor available for guidance. If you can develop labs that interest the student the level of effort and the amount learned increases. The course was developed to include 8 laboratory assignments which work together to complete the display system. In addition homework, quizzes, a midterm and final are used to evaluate the students level of understanding.

The midterm asks the students to solve design problems by following basic design steps and implementing the solution using VHDL. Questions requiring both debug skills and coding skills are asked.

The final exam grade was 50% traditional examination similar to the format of the midterm and 50% oral presentation on a topic of interest related to FPGA or ASIC design.

Lectures include examples where the solution is presented in a five step (analyze, design, code, debug, and test) approach. All problems (lecture examples, lab assignments, and examination questions) are selected to illustrate common situations encountered by engineers.

Mid Term Exam	20%
Final Exam	20%
Laboratory Grade	40%
Weekly Quizzes / Homework Assignments	20%

The following check list was used for correcting and grading laboratory assignments and tests.

Internal Code Format and Style

During the first week of class the Coding guidelines were reviewed with the students. The document was then used to check for the following main points when the lab was graded.

- Does the program include a comment block with the author's name, program creation data, and anti-plagiarism statement?
- Are signal and variable names descriptive and appropriate?
- Are comments used to aid in the understanding of the code?
- Is white space used to improve the readability of the program?
- Are indents used properly to denote IF/FOR/ELSE/…. Statements?
- Are begin and end statements aligned properly?
- Are the steps followed for analysis and design documented clearly?
- Is the lab signed off proving that the instructor or lab TA witnessed the design functioning properly?

Accompanying Documentation

- Is the lab report documentation neat, and professional?
- Are all the in lab measurements clearly formatted with the appropriate headings?
- Does the lab report have a cover page, results and conclusion section.

Summary

Rochester Institute of Technology requires a course in Principals of Design Automation for Electrical Engineering Technology and Computer Engineering Technology students. At the completion of the course, students are expected to know the basics of coding for synthesis, test bench techniques, modelsim simulator, and the Xilinx tool flow for targeting complex programmable logic devices (CPLD's) and field programmable gate arrays (FPGA's). The prerequisites are Digital System Design and a formal, structured programming course.

To successfully meet the learning objectives of the course, an eight lab sequence which creates a digital display system in eleven weeks was developed. The students are now excited to come to lab and are working hard because they enjoy the project. In addition to the design knowledge the student also learns the basics of configuration management, team dynamics, communication, and ethics.

The plans for the future include the integration of a VGA Camera, the integration of a low cost ceramic speaker, and a textbook to support the design and verification of the project. In addition a course which covers Verilog and System Verilog. Finally integrate a linting tool into the course to help enforce the coding guidelines.

References

1. Avnet Design Services, Xilinx Spartan IIE Evaluation Kit. Literature # ADS002704

Author Biography

Jeff Lillie is a design engineer with a BSEE (1988) from Rochester Institute of Technology, and a MSEE (1993) from the University of Rochester in Image Processing. He is an IC Design engineer at National Semiconductor(**http://www.national.com/appinfo/displays/**) in the small format displays division. In addition he is an assistant professor at the Rochester Institute of Technology Computer Engineering Technology Department.